# Trigger Electronics Upgrade of PHENIX Muon Tracker

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**Abstract**

The Relativistic Heavy Ion Collider (RHIC) at Brookhave National Laboratory (BNL) provides a unique opportunity to collide polarized protons at high energies. One of the hightlights of the polarized proton program at $\sqrt{s}$ = 500 GeV is the direct measurement of sea quark contribution to the proton spin via $W$-boson production by measuring parity violating single spin asymmetry. A new trigger electronics on forward muons which specializes in $W$-boson detection was developed for the PHENIX experiment. The trigger was installed as an additional electronic circuit which is connected in parallel to existinig cathode readout elecctronics of the muon tracking chamber.

*Keywords:*

## 1. Introduction

A new trigger on forward high-momentum muons for the PHENIX experiment was developed for the purpose of measuring longitudinal spin asymmetry in $W$ boson production at polarized proton-proton collisions with $\sqrt{s}$ =500 GeV at RHIC. The measurement provides a direct probe to the individual polarized parton distribution function (PDF) of the quarks and anti-quarks in the proton. Since the muon trigger before the upgrade fired on any muons above 2 GeV/$c$, it was inefficient to trigger high-momentum muons from $W$ decays and did not provide the required trigger rejection factor for 500 GeV running. The new system performs coarse online tracking and triggers events with high-momentum particles by selecting straight tracks in a magnetic field. It suppresses a large number of background events of low momentum muons coming from hadronic decays. Three major upgrade projects are parts of the new trigger; (1) Resistive plate chambers (RPC1 and RPC3) [2], (2) Upgrade of muon tracker front-end electronics (muon trigger front-end electronics, MuTRG-FEE) [3], (3) Additional hadron absorber. We discuss (2) in this article.

### *1.1. Physics motivation*

Parity-violating production of the $W$ boson with longitudinally-polarized proton-proton collisions at RHIC provides a direct measure of the individual polarizations of the quarks and anti-quarks in the colliding protons. The high energy scale set by the $W$-mass makes it possible to extract quark and anti-quark polarizations from inclusive lepton spin asymmetries in $W$-production with minimal theoretical uncertainties. Sub-leading twist and higher-order terms in the perturbative QCD expansion are strongly suppressed, and a direct extraction without additional assumptions becomes possible [1]. This program thus will break new ground in our detailed understanding of the proton's structure. Especially, our present knowledge for the anti-quark contribution to the proton spin is limited with larger uncertainties to measurements by semi-inclusive deep-inelastic scattering (SIDIS). In addition to forementioned naturally set high energy scale, the sea quark measurement via $W$ has certain advantage with respect to SIDIS in following sense: 1) The $W$ boson couples with the quark flavor selectively, and quarks (anti-quarks) with negative (positive) helicity can participate in the reaction due to the V−A structure of the weak interaction, 2) free from fragmentation function which is the unavoidable dominant source of model uncertainties for SIDIS on their way to extract the sea quark polarization from observed asymmetries. Because the measurement of $W$ asymmetry in forward/backward angle give large probability of kinematics of unbalanced Bjorken $x$'s from two colliding protons, the measurement of $W$ asymmetry in forward/backward angle further enhances the sensitivity to the sea-quark polarization.

The $W$ program was initiated by the first operation of RHIC polarized proton beams at its highest operational energy $\sqrt{s}$ =

500 GeV in 2009. This $W$ program is the highlight of RHIC spin project for the next five years and thus following upgrade projects to PHENIX muon arms have been pursued to prepare for the rare probe measurement under high-background rate circumstances.

### *1.2. RHIC polarized proton beam*

RHIC [4] consists of two counter rotating accelerator/storage rings with six beam crossings points labeled as 2,4,6,8,10, and 12 o'clock where collisions may take place. Each rings are built on a common horizontal plane, one ("Blue Ring") for clockwise and the other ("Yellow Ring") for counter-clockwise beams. Each RHIC ring is capable of being loaded with 120 bunches at maximum with optional spin direction. RHIC operated with up to 112 bunches filled and with consecutive eight missing bunches at the end of the bunch train in the 2011 RHIC Run. The revolution frequency of RHIC is 78 kHz and bunches are spaced by 106 nsec apart. This timing pulse is called the RHIC beam clock and distributed to experiments in order to let readout system of detectors to be synchronized with the collision timing.

### *1.3. PHENIX and preexisting muon arm detector*

The PHENIX detector [6] is a large multipurpose set of detectors optimized for measuring rare electromagnetic probes (photons, muons, and electrons) of the spin structure of the proton and of the hot dense matter created in ultra-relativistic heavy ion collisions. The data acquisition system and multi-level triggers are designed to handle the largely different challenges presented by $p+p$ collisions (relatively small data size per event at very high rates) and Au+Au collisions (very large data size per event at relatively low rates) with little or no dead time [7, 8]. Event characterization devices, such as the Beam-Beam Counters [9], provide information on the vertex position, start time, and centrality of the collision. The two muon arms, shown in Fig. 1, which specialize in muon detection cover $1.2 < |\eta| < 2.4$ in pseudorapidity and $\Delta\phi = 2\pi$ in azimuth which results in acceptance of almost 1 sr.

The Beam-Beam Counters (BBCs) [9] each consist of 64 quartz radiators instrumented with mesh dynode PMTs and arranged in a cylinder coaxial with the beam. The BBCs are placed on either side of the collision vertex and cover $3.0 < |\eta| < 3.9$. Each channel has a dynamic range extending to 30 MIPs. The BBCs measure the arrival times of particles on both sides of the collision vertex. From the average of these times we determine the event start time. From their difference we obtain the position of the vertex along the beam direction. The BBCs also provide the minimum-bias interaction trigger, which requires that there be at least one hit in each BBC.

The muon arms [5] are coaxial with the beam on opposite sides of the collision vertex. The two arms which are located on the south and north end of the interaction region are named for convention as "South arm" and "North arm", respectively. Each muon arm is comprised of a Muon Tracker (MuTr) and a Muon Identifier (MuID). The MuTr makes an accurate measurement of particle momenta. The MuID allows coarse resolution track reconstruction through a significant amount of steel

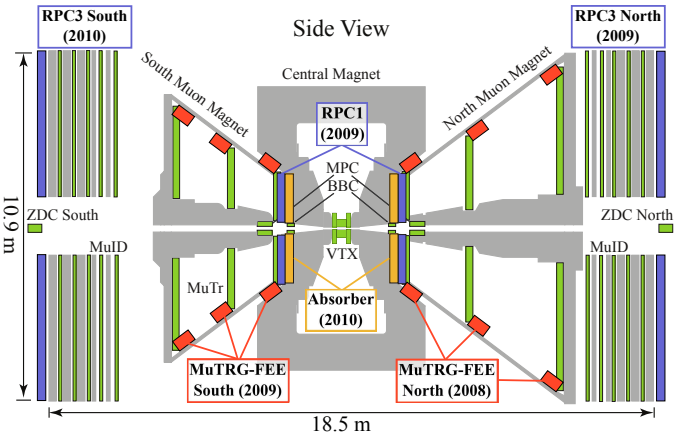



Figure 1: The PHENIX muon arm detection system and new devices to upgrade the trigger performance of the muon arms. New devices are given their names and year of the (scheduled) installation.

absorber. Before reaching the MuTr detectors a particle must pass through the pre-MuTr absorber; 20 cm of copper (named as nosecone) plus 60 cm of iron (part of the MuTr magnet).

Each MuTr arm consists of three stations (named Station-1, Station-2, and Station-3 proceeding downstream from the collision vertex) of cathode-readout strip chambers. They are installed in an eight-sided conical magnet [10] which provides the radial magnetic field ( $\int \mathbf{B} \cdot \mathbf{dl} = 0.72\,\mathrm{T{\cdot}m}$ at 15 degrees, $B(\theta) \approx B(15^\circ)\tan(\theta)/\tan(15^\circ)$) and bends particles in the azimuthal direction. Each MuTr station occupies a plane perpendicular to the beam axis and also partitioned into identical eight segment called "octant". The octant consists of multiple ionization gaps of an anode plane sandwiched by two cathode planes; three gaps for the two stations closest to the collision vertex and two gaps for the last station. The anode planes are alternating structures of 20 $\mu$m-diameter gold-plated tungsten sense wires and 75 $\mu$m-diameter gold-plated copper-beryllium field wires. Each wire is running along the azimuthal direction with a sense wire spacing of 10 mm. Cathode planes are segmented into strips of 5 mm pitch with readout alternately. Half of the cathode planes have strips oriented perpendicular to the anode wires (non-stereo planes) and the other half have strips with a small stereo angle of 11.25 degree or less (stereo planes) to provide two-dimensional information. The chamber gas mixture is 50 % Ar + 30 % $CO_2$ + 20 % $CF_4$. Typical operating high voltage is 1900 V with a gain of approximately $2 \times 10^4$. An ionizing particle typically fires three adjacent strips in each orientation to form "cluster". A fit to the charge profile on the cluster provides a position measurement with a designed resolution of about 100 $\mu$m in the bend direction.

Each MuID arm consists of five steel absorber plates interleaved with Iarocci tubes[14] operated in proportional mode and specialized shielding to reduce backgrounds not originating from the collision vertex. The first MuID absorber plate (thickness = 20 cm - South; 30 cm - North) also serves as the return yoke of the MuTr magnet. Successive plates (identical for the two arms) are 10, 10, 20 and 20 cm thick, thus totaling

$4.8\lambda_I/\cos\theta$ ($5.4\lambda_I/\cos\theta$) for the South (North) arm, where $\lambda_I$ indicates the nuclear interaction length and $\theta$ is the polar angle of a particle's trajectory. Gaps are labeled 0 to 4 proceeding downstream from the collision point. Each gap consists of horizontal and vertical Iarocci tubes with ~8 cm width and 2.5 – 5 m length to provide coarse two-dimensional position. Tracks which penetrate all MuID steel plates and point to the collision vertex are identified online and triggered as conventional PHENIX muon arm trigger.

### *1.4. Trigger upgrade*

#### *1.4.1. Overview*

The trigger for the muon arms before the upgrade was generated by MuID. It provides the rejection power of ~200 compared with the PHENIX minimum-bias trigger by BBC at $\sqrt{s}$ = 200 GeV.[1] The RHIC design goal of the luminosity is $2.0 \times 10^{32}\mathrm{cm}^{-2}\mathrm{s}^{-1}$, which results in about 6 MHz of BBC trigger. In order to meet the typical DAQ bandwidth of 2 kHz for the PHENIX muon arm, the rejection power of 3000 is required. Based on a prediction that the rejection power by MuID will not be so much different between 200 GeV and 500 GeV, the MuID trigger wouldn't be sufficient to trigger $W$ without pre-scaling.

The momentum threshold of the MuID trigger is $p_T \sim$ 1.5 GeV/$c$, while the typical muons decay from $W$ boson dominates the single muon yields at high transverse momentum region $p_T \gtrsim 15$ GeV/$c$ with respect to background muon sources as shown in Fig. 2. Based on this fact, raising the threshold even higher leads to the efficient trigger of the signal with sufficient rejection power. Here we introduced a new momentum-sensitive trigger by adding new fast readout electronics (muon trigger front-end electronics, MuTRG-FEE) to existing MuTr front-end electronics. MuTRG-FEE digitize the signal immediately and therefore deal with only hit information providing fast and coarse online tracking information of the traversing particle in MuTr to back-end trigger logic circuit. Events with high-momentum charged particles are triggered based on the online tracking results.

However, due to the limited intrinsic timing resolution of MuTr (approximately 2 – 3 beam clocks), the other timing detector with sufficient timing resolution is needed to identify the beam clock which collision bunch an observed hit comes from. BBC can be such a timing detector and we evaluated MuTRG-FEE performance in collaboration with BBC for this article. However, the situation will be more serious at high collision rate where BBC will start triggering every events and will not determine collision timing. Another new upgrade detector, resistive plate chambers (RPC), will resolve the difficulty taking advantage of its sufficient intrinsic timing resolution of a few nsec and low occupancy owing to its small segmentation. If one finds corresponding hit in the RPC at the expected location from the extrapolation of the track observed by MuTRG-FEE, the timing observed by RPC is allocated to the track.

[1]We define the trigger rejection power as the number compared to the PHENIX minimum-bias trigger rate by BBC in this article. The cross section observed by BBC is about 30 mb at $\sqrt{s}$ = 500 GeV, which is about half of the proton-proton total cross section.

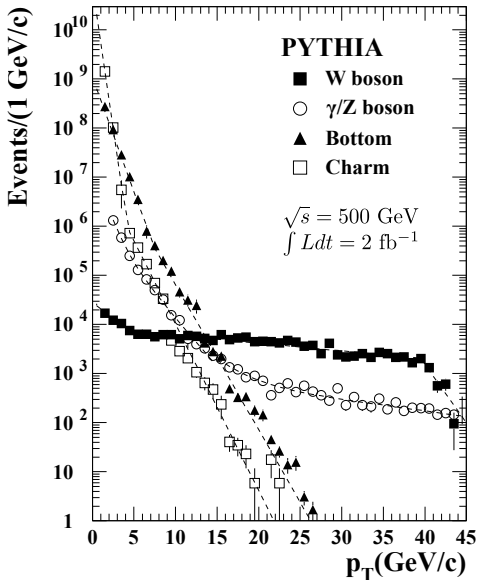



Figure 2: Expected inclusive muon spectrum at $\sqrt{s}$ = 500 GeV plotted as a function of transverse momentum $P_T$ of muon simulated by PYTHIA.

#### *1.4.2. MuTRG-FEE*

Fig. 3 displays the principle of selecting high-momentum particles by MuTRG-FEE. Δstrip is introduced to be an important parameter to identify high-momentum tracks and is defined as a deviation of hit at Station-2 from the linear interpolation between Station-1 and Station-3 hits. In this article, we use Δstrip in the unit of the number of strips. Selecting events which have tracks with small Δstrip, e.g. $|\Delta\mathrm{strip}| \leq 1$, the new electronics provides the trigger of only high-momentum track.

A block diagram of the new muon trigger system is shown in Fig. 4. A new amplifier and discriminator board (MuTRG-ADTX) are attached to MuTr front-end electronics (MuTr-FEE) and divides the signal into two paths; analog readout path for existing MuTr-FEE and the digitization path for the fast trigger. The digitized signals are sent to new data merger boards (MuTRG-MRG), which are located in the PHENIX rack room and about 70 m far from the collision region. The MuTRG-MRG board collects hit signals from multiple MuTRG-ADTXs and formats the data to meet the input format of the downstream Local Level-1 (LL1) trigger module. To identify tracks which fire the trigger in the offline analysis, the copy of hit patterns transmitted to LL1 from MuTRG-MRG is sent to data collection modules (DCM) via other interface boards (MuTRG-DCMIF). The data are then recorded into PHENIX main data stream. We name MuTRG-FEE as a system which consists of MuTRG-ADTX, MRG and DCMIF. The LL1 module makes trigger decision by comparing hit patterns from MuTRG-MRG and pre-defined look-up table which contains hit combination of high-momentum tracks. The signals from other upgrade detectors, RPCs, can also be merged in the LL1 module. The local trigger decision by LL1 module is finally transmitted to the Global Level-1 (GL1) trigger module, where the PHENIX global trigger is generated in combination with LL1 triggers

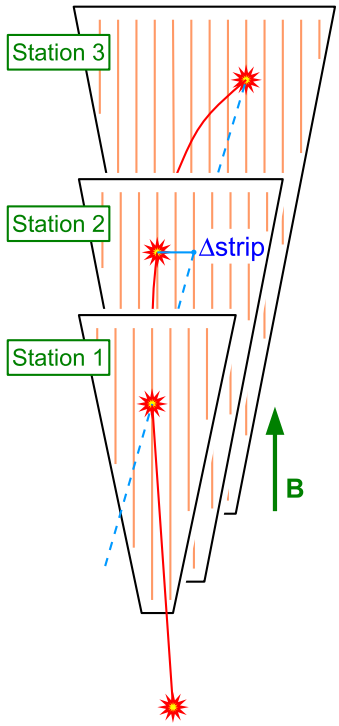



Figure 3: The concept of momentum-sensitive trigger using muon tracker cathode strip readouts. A coarse momentum measurement is carried out online by calculating Δstrip, a deviation of hit at Station-2 from the linear interpolation between Station-1 and Station-3 hits. Tracks with small Δstrip are triggered.

from other detector systems like MuID and BBC.

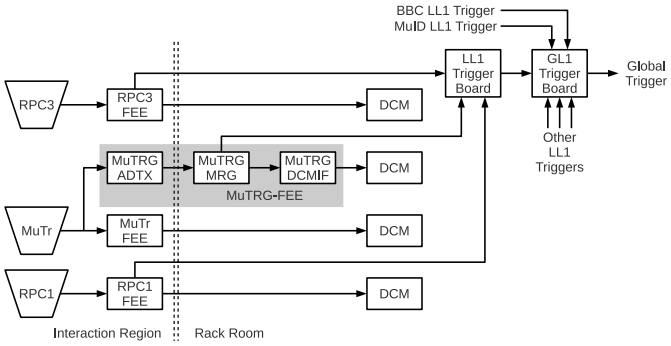



Figure 4: The block diagram of the new muon trigger system.

The R&D of these new boards were completed by the end of 2008. The production and installation to North muon arm was completed in 2008 and they were commissioned in the 2009 RHIC Run, whereas South muon arm was completed in 2009 and were commissioned in the 2010 RHIC Run Au-Au collision data as well.

### *1.4.3. Resistive plate chambers*

The PHENIX resistive plate chamber (RPC) has a standard double gap structure and is based on the RPC's built for the Compact Muon Solenoid (CMS) experiment at CERN. The gas chamber is constructed with two 2 mm bakelite plates ($\sim 10^{10}$ Ω cm), as resistive plates, with 2 mm gap. The outside surface of the RPC is coated with graphite, which are used as electrodes. A high voltage of −9.5 kV is applied to one side of the graphite and the other side is grounded. Readout planes are made from copper strips running along the azimuthal direction to measure an azimuthal position which is sensitive to the track momentum. Gas is 95% $C_2H_2F_4$ + 4.5 % i-$C_4H_{10}$ + 0.5 % $SF_6$. One of the attractive features of the RPC detector is that the readout plane is completely isolated from the gap chamber. Charge is induced on the readout strip by an avalanche in the gas gap and processed by the readout electronics. Some features of the PHENIX RPC as the new *W* trigger are listed on Table 1.

Table 1: Characteristics of the PHENIX RPC with −9.5 kV supplied.

| PHENIX RPC characteristics | |
|---|---|
| Cluster size | <2 strips |
| Efficiency | >95 % for MIP |
| Time resolution | ~2 nsec |
| Rate capability | 0.5 kHz/cm$^2$ |
| Segmentation | <1 degree in azimuth |

Owing to the good timing resolution, RPC plays an important role as a timing device under the high luminosity circumstances substituting for BBC, as well as it provides a strong suppression against cosmic-ray background. RPC prototype was partially installed during RHIC shutdown period in 2008 and commissioned in the 2009 RHIC run with beam collisions. RPC installation behind MuID (RPC3) for both muon arms were completed in the RHIC shutdown period of 2009 and 2010. Additional RPC installation in front of MuTr (RPC1) is being carried out in the 2011 RHIC shutdown period.

### *1.4.4. Additional hadron absorber*

Another piece of the upgrade is a new hadron absorber which is mounted downstream of the MuTr magnet. The 35 cm-thick SS310 absorber plates with 24 tons were manufactured at ATLAS Tool&Die Works, Lyons, IL, USA on contract from the University of Illinois at Urbana-Champaign, USA. SS310 is Cr (24 – 26%) and Ni (19 – 22%) enriched austenite phase stainless steel. It has characteristic of small magnetic permeability of $\sim 10^{-3}$ and thus makes minimum impact to well measured existing magnetic field. By installing the new absorber, the pre-MuTr absorber presents a total thickness of $7.1\lambda_I/\cos\theta$ (was 4.9 before), where $\theta$ is the polar angle of a particle's trajectory. This absorber reduces the MuTr occupancy and provides the first level of hadron rejection of a factor of about three orders of magnitude. Due to ionization energy loss, a particle must have a momentum at the vertex which exceeds $2.71/\cos\theta$ GeV/$c$ ($2.85/\cos\theta$ GeV/$c$) to penetrate to the most downstream MuID gap of the South (North) arm after new absorbers are installed.

## 2. MuTRG-ADTX board

MuTRG-ADTX boards are located just next to MuTr and attached to existing MuTr-FEE to deal with raw signal from MuTr. The signals are digitized in this board to generate fast signal for the Level-1 trigger. Main functions of MuTRG-ADTX are followings.

- Splitting charge from MuTr to two paths, MuTr-FEE and MuTRG-ADTX.
- Amplifying and discriminating raw signals.
- Formatting digitized signals to transmit them to the downstream MuTRG-MRG board via an optical cable.

MuTRG-ADTX was developed based on two important guideline. One is to minimize impact on performance, position resolution and detection efficiency, of existing MuTr-FEE. Since the momentum resolution of a detector like MuTr is increasing quadratically as the momentum of the particle becomes higher, it is important to keep the MuTr resolution as better as possible for $W$-boson detection. The other guideline is to process MuTr signal fast enough to be in time for the trigger decision with high efficiency and good timing resolution. A restriction in the development is that any components affected by magnetic field are unavailable because MuTRG-ADTX is installed inside or attached to the muon arm filled with magnetic field. The specification of MuTRG-ADTX and its chassis are summarized in Table 2.

### *2.1. Analog part*

MuTRG-ADTX is designed to consume minimal portion of the signal charge from MuTr to form the trigger primitives, leaving a large fraction of the charge for the MuTr-FEE to save the gain as much as possible. A small capacitor of 56 pF ($C_{split}$) is implemented to divide the charge at the input of MuTRG-ADTX as shown in Fig. 5. Because effective capacitance of the existing MuTr-FEE is about 900 pF, about 5 % of the charge from MuTr is transmitted to MuTRG-ADTX and the remaining 95 % of the charge is used by existing MuTr-FEE to provide precise position information. On the other hand, the additional capacitance could behave as the new noise source on MuTr-FEE. The small capacitance for the $C_{split}$ is preferable in this sense. Cables connect between MuTRG-ADTX and MuTr-FEE were employed as short as 30 cm for the most of part from the same reason above. Another impact of $C_{split}$ on MuTr-FEE is delay of signal timing. These impact on MuTr-FEE is evaluated in Section 3.1.

The raw signals are amplified and discriminated there and sent to the digital part of MuTRG-ADTX as the second stage. Fig. 6 shows the circuit diagram of the MuTRG-ADTX analog part. Since a typical charge deposit on MuTr by a single charged particle is 100 fC and only about 5 fC can be available in MuTRG-ADTX, low noise and high gain are preferable. On the amplifier part, we selected AD8038 and AD8065 op-amp of Analog Devices which feature high speed and low noise. Pulse height and peak time after the amplifier is about 300 mV and

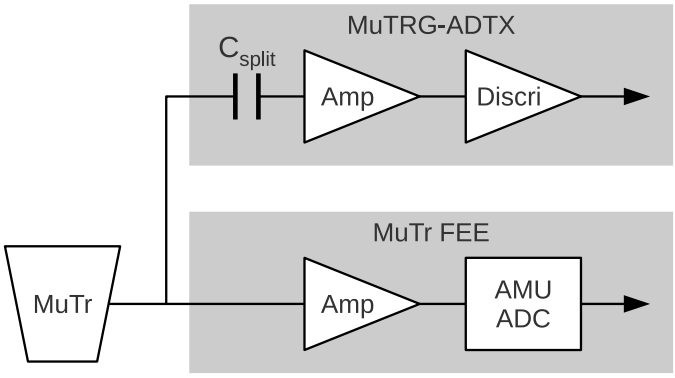



Figure 5: Schematic diagram of the charge split between MuTr-FEE and MuTRG-ADTX.

200 nsec with 100 fC charge deposit in MuTr. Noise after the amplifier is about 5 mV in root-mean-square (RMS).

For the discriminator part, we implemented cable-less constant fraction discriminator (CFD) to eliminate time walk effect as well as nominal leading edge discriminator (LED). CFD is realized by producing high-pass and low-pass signal from the original signal and transmitting them to comparator (See also Fig. 7). The output signal timing of the comparator is determined by the intersection of high-pass and low-pass signal, which is independent of the pulse height. LED is also generated by another comparator with the original signal and threshold voltage as inputs. The threshold voltage are provided by 8 bit DAC (Digital-to-Analog Converter) with a range of 0 to 125 mV. Because the timing of the CFD output always delays by about 250 nsec than the LED output, the timing of the AND signal of the CFD and LED signal is determined by that of the CFD signal, as well as its threshold is equivalent to that applied to the LED signal. In the following text, We describe CFD as the signal after taking AND of LED and CFD for convenience.

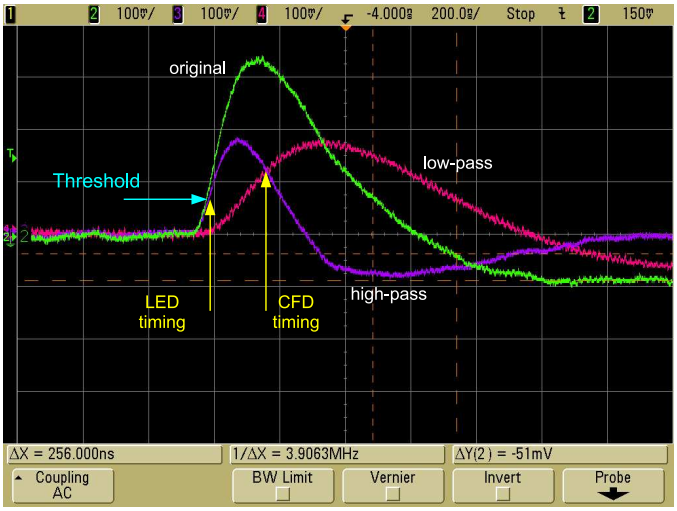



Figure 7: Signal shape used for CFD. Measured at test bench.

MuTRG-ADTX board consists of 8-layer substrate and use

Table 2: Specification of ADTX and chassis of ADTX.

| ADTX | |
|---|---|
| Board Size | 6 U |
| Number of channels | 64 at maximum |
| Supplied Low Voltage | 6.2 V (5.7 V at minimum) |
| Used Voltage | 5.25, 3.3, 2.5, 1.25 V (modulated by regulators) |
| Consumption Current | ~2.0 A |
| Power Consumption | ~12.4 W |
| Signal Process Time | 2.5 – 3.5 beam clocks with LED |
| | 5.2 – 6.2 beam clocks with CFD |
| **Chassis of ADTX** | |
| Size | $189 \times 267 \times 36$ mm$^3$ |
| Capacity | 2 boards |
| other features | Water cooling and dry air supply system are equipped. |

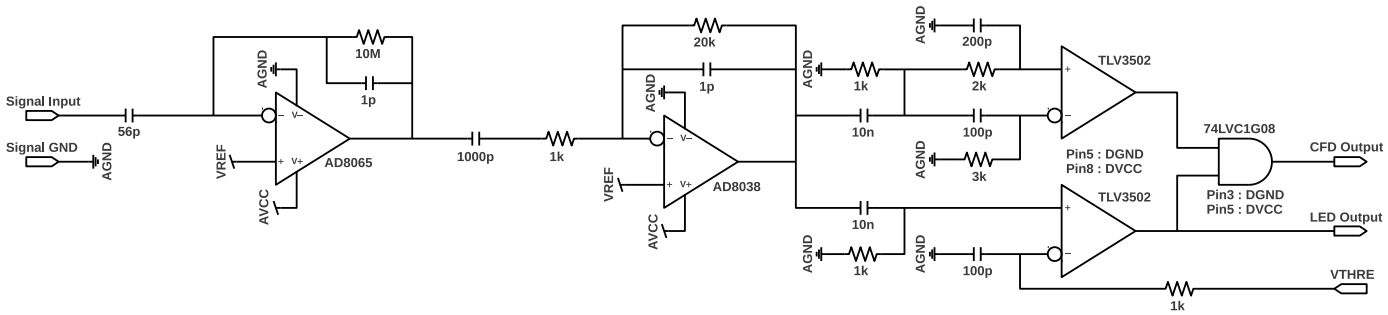



Figure 6: The circuit diagram of MuTRG-ADTX analog part. AGND and DGND represents analog and digital ground, respectively. AVCC, DVCC and VREF are 5.25 V, 3.3 V and 1.25 V, respectively. VTHRE indicates threshold voltage for the analog signal.

of each layer is summarized in Table 3. Although the ground of analog sector (AGND) and that of digital sector (DGND) have electrical conduction via ground of voltage regulators, they are well separated to prevent the noise generated in the digital sector picked up in the analog sector. The first and the last layer is used for frame ground (FGND) and FGND has electrical conduction with chassis of MuTRG-ADTX. We have option of making AGND/DGND and FGND common or not. Finally we decided common ground for AGND/DGND and FGND to obtain stable ground. In addition, we made common ground for MuTRG-ADTX chassis, shield line of the signal cable from MuTr and MuTr-FEE chassis.

Table 3: Layers of MuTRG-ADTX. Components are mounted on both the first layer and the 8th layer.

| Layer number | Layer user |
|---|---|
| 1 | FGND |
| 2 | AGND and DGND (separate) |
| 3 | Signal |
| 4 | AGND and DGND (conducted) |
| 5 | Signal |
| 6 | AGND and 3.3 V |
| 7 | 1.25 V, 2.5 V, 5.25 V and supply voltage |
| 8 | FGND |

The size of MuTRG-ADTX board is nearly 6U and 2 boards can be contained in one chassis. Fig. 8 is the picture of MuTRG-ADTX board. Each board is capable of processing up to 64 inputs. To avoid possible cross talk between adjacent channels, signal lines are located in parallel with each other and analog and digital part are located separately at top and bottom region in Fig. 8. The maximum required voltage for ICs in MuTRG-ADTX is 5.25 V and minimal required supply voltage is measured to be about 5.7 V. The operating voltage was tuned to be 6.2 V at the board introducing the safety factor of 0.5 V. The current draw is about 2 A and resulting power consumption is calculated to be 12.4 W per board. The chassis has water cooling structure in both sides which keeps the inside below 60 degrees by continuous flow of cooling water. In addition, heat sink are attached to the significant heat source, i.e. regulators.

### *2.2. Digital part*

The main function of the digital part of MuTRG-ADTX is serialization of the input signal. The 64-bit input signal is digitized, serialized and then transmitted to downstream MuTRG-MRG via an optical cable.

Analog signal is converted to digital hit information with a threshold set by DAC (Digital-to-Analog Converter; MAX5259, MAXIM), which is controlled by FPGA (Field Programmable Gate Array; Spartan3, XC3S1000, Xilinx). The

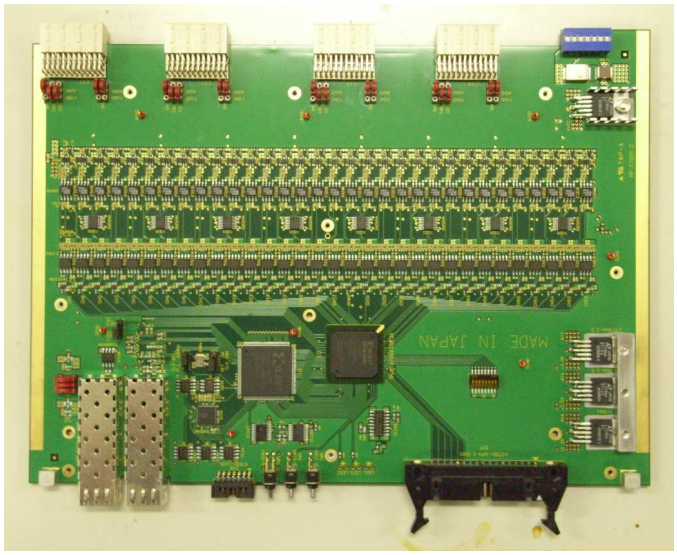


Figure 8: The picture of MuTRG-ADTX board.

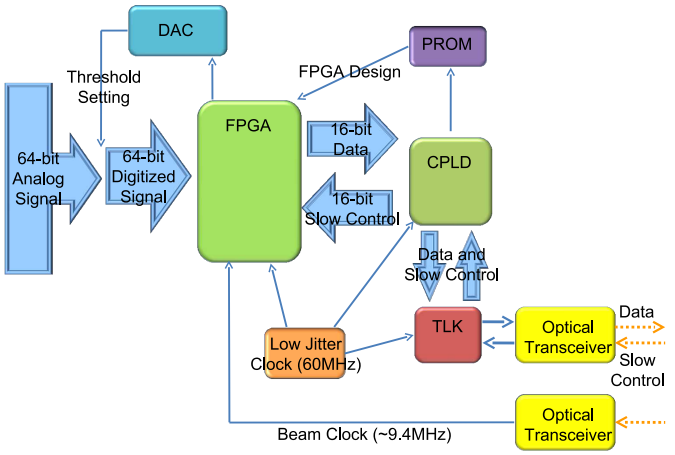



Figure 9: The block diagram of the digitized data flow. The main function of the digital part of MuTRG-ADTX is serialization of the input signal. The 64-bit input signal is digitized, serialized and then transmitted to MuTRG-MRG via an optical cable. The data stream is processed by FPGA, CPLD, TLK, and optical transceiver. CPLD also plays important role in slow control.

digitized 64-bit signal is transmitted to FPGA at a rate of the beam clock of ~9.4 MHz (106 nsec) as it synchronizes with beam collision. For the operation synchronized with the collision rate, the RHIC beam clock is distributed to all MuTRG-ADTX via dedicated optical fibers beside the forementioned data transfer line.

The 64-bit parallel signal in FPGA is reformatted into six sequential 16-bit data including footers. This reformat is necessary to utilize TLK1501 (Texas Instruments) which only has 16 input pins. TLK1501 is a serializer and equipped in order to adjust the signal to the input of optical transceiver (AFBR5710LZ, AVAGO). In the process of the reformatting, asynchronous clock of 60 MHz is used since TLK1501 requires clean clock with jitter of 40 psec in peak to peak, whereas the jitter of the RHIC beam clock is about 25 psec in RMS. The asynchronous process is realized at FIFO (Fast In Fast Out) modules inside the FPGA and more detail about this system is described in Section 2.3. The reformatted 16-bit data are transmitted at the speed of 1.2 Gbps as a serialized optical signal. This rate is a consequence of 8b/10b encoding implemented in TLK1501 (16 bit $\times$ 60 MHz $\times$ 10/8 = 1.2 Gbps).

Fig. 9 illustrates the block diagram of the digital part of MuTRG-ADTX. CPLD (Complex Programmable Logic Device; XC95144XL, Xilinx) and PROM (Programmable Read Only Memory; XCF04S, Xilinx) are equipped for slow control which is described in Section 2.4.

### *2.3. FPGA*

FPGA plays important roles in the threshold setting and the asynchronous data reformat. Threshold values of 64 channels can be controlled independently. The threshold voltage ranges from 0 to 125 mV and the value can be set in ~0.5 mV step. The values are written in RAMs inside the FPGA and loaded to the daisy-chained eight DAC chips (one DAC distributes to eight channels). There are two modes in slow control for the threshold setting. One is a threshold writing to the RAM and the other is a threshold loading (see Section 2.4). The loaded threshold values can be monitored by hit rates which are recorded and displayed in the online monitor during data taking.

Fig. 10 displays the function of FPGA, reformatting the 64-bit parallel data into transmit-ready format via the optical transceiver. The breakdown of the reformatted data is; 1st-4th are input signal, 5th is beam clock counter (8-bit) + board ID (8-bit) and 6th is Carrier Extender (C.E.) which defines the boundary of the data of a given beam crossing. FIFO is used in the FPGA to realize the asynchronous process. The frequency of input clock for the FIFO is about 56.6 MHz which is made by PLL (Phase Locked Loop) inside the FPGA from RHIC beam clock multiplied by six (1 / 106 nsec $\times$ 6 ~ 56.6 MHz). This rate is determined in order to transfer six sequential packets in just proportion. The output clock for the FIFO is distributed from a crystal clock (KC5032C-C3, KYOCERA) located at outside of the FPGA. This clock must be faster than 56.6 MHz not to drop off any data, therefore 60 MHz model was employed which meets the requirement and available in the market. The jitter of the crystal clock is 40 psec in peak to peak and satisfies the jitter requirement of TLK1501 (40 psec in peak to peak). In summary, this asynchronous process switches the operating clock from RHIC beam clock to the crystal clock and enable us to operate the TLK1501 located at the downstream of the FPGA.

As a result of the inconsistent frequencies between the input and output clock of the FIFO, MuTRG-ADTX ends up sending empty packets of 3.4 MHz (= 60 − 56.6) to its downstream. These packets are however ignored in MuTRG-MRG.

### *2.4. Slow control*

As it is essential to control functions of MuTRG-ADTX remotely during the beam time, several slow control capabilities are implemented in MuTRG-ADTX. The slow control signal is

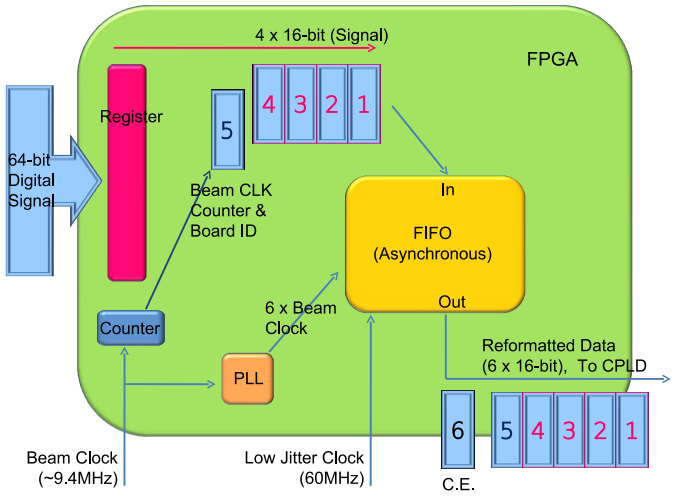



Figure 10: The block diagram of the logic of the data reformat in the FPGA. The 64-bit input signal transmitted to the register is divided into four packets by the clock of 56.6 MHz (6 × RHIC beam clock). These four packets are transmitted to the FIFO with 5th packet (beam clock counter (8-bit) + board ID (8-bit)) by the same clock. Then, those packets are read out asynchronously by the crystal clock of 60 MHz. This asynchronous process switches the operating clock from the beam clock to the crystal clock and enable us to operate the TLK1501 located at the downstream of the FPGA. The 6th packet (C.E.) is added at the input of the FIFO by 56.6 MHz.

transmitted from MuTRG-MRG via optical cables to prevent possible noise source for the analog signal. CPLD serves an important role in slow control and receives 16-bit control signal via TLK1501 (Fig. 9). There are two categories of slow control mode. The first one is targeting the FPGA and the second one is targeting the PROM. The target device is identified in CPLD based on a few digits from MSB (Most Significant Bit) of the received 16-bit.

The first category of the slow control includes two writing modes and contents are the following;

- Data transfer mode
- FPGA reset
- Test pulse transfer mode
- Writing test pulse pattern
- Threshold loading
- Writing threshold values

Data transfer mode activates the FPGA function and hit data sent to MuTRG-ADTX is transmitted to MuTRG-MRG. FPGA reset mode initializes the modules in the FPGA (register, beam clock counter, PLL, FIFO). Test pulse transfer mode is useful for debugging purpose. It generates pre-programmed signal internally which enables us to test the digital part of MuTRG-ADTX without having the signal input from the analog part. The test pulse patterns are also written in RAMs inside the FPGA like the threshold values and up to 4 patterns of 64-bit can be stored at most. The detail of the threshold setting is described in Section 2.3.

The second category is writing the FPGA design to the PROM. The FPGA design is transmitted in JTAG protocol from MuTRG-MRG via an optical cable and written to the PROM [12]. The design is loaded to the FPGA automatically when MuTRG-ADTX power is turned on.

### *2.5. Production and installation*

Then mass production of MuTRG-ADTX boards were carried out in Japan, then they were shipped to BNL. All 400 boards, including 10 % spare boards, were tested both at RIKEN, Japan and BNL, US before installation using test pulse. The items examined by the test are listed below.

- Gain reduction on MuTr-FEE
- Channel-by-channel cross talk
- Fake hit rate
- Efficiency
- Slow control (reset, threshold setting, PROM configuration)

Failure was detected in 13 boards out of 400 boards in total by this test. Most of the failure mode include broken chip and soldering failure. Finally all boards passed the examination after fixing the problem.

The board production were performed in two periods depending on the installation schedule. MuTRG-ADTX were installed during RHIC shutdown period in 2008 for the North MuTr and in 2009 for the South MuTr. The installation was carefully performed not to damage existing system and to avoid mis-cabling because we had to disconnect cables between MuTr and existing MuTr-FEE to attach MuTRG-ADTX. We also checked noise on MuTr-FEE, which directly affect position resolution of MuTr. After the installation we examined the MuTRG-ADTX performance with calibration pulse by controlling them using MuTRG-MRG and confirmed all boards worked properly.

## 3. MuTRG-ADTX performance

The performance of MuTRG-ADTX can be separated into two components; (1) Impact on the existing MuTr-FEE and (2) Performance of MuTRG-ADTX itself. We evaluated the performance of MuTRG-ADTX in several test experiments with beam as well as with cosmic ray and test pulse at a test bench. The results in the following sections include those from such various measurements. Here are the list of such measurements.

- Test bench at Kyoto University and RIKEN with test chamber
- An electron beam test at Tohoku University in 2006
- A cosmic ray test at PHENIX in 2007
- A beam test at PHENIX in 2008 (200 GeV *p*-*p* collision)

- A beam test at PHENIX in 2009 (500 GeV *p*-*p* collision)
- A beam test at PHENIX in 2010 (200 GeV/u Au-Au collision)
- A beam test at PHENIX in 2011 (500 GeV *p*-*p* collision)

Since the development of MuTRG-ADTX had been in progress, the MuTRG-ADTX boards used in those measurements were not identical. The development of the board started with analog and digital part separately to avoid possible noise from digital part to analog part and to make easier to figure out the source of the problem. The board of analog and digital part is named as MuTRG-AD and MuTRG-TX, respectively. Based on the first measurement at the PHENIX detector and confirmation that digital part didn't affect the performance of analog part, a significant upgrade of combining analog and digital part was decided between two measurements in 2007 and 2008. The final design was fixed after the test measurements in 2008.

### *3.1. Impact on the existing MuTr-FEE*

#### *3.1.1. MIP distribution*

MuTr readout system records four ADC sample for each signal as shown in Fig. 11. By fitting the four points to quadratic function, pulse height and signal timing can be extracted.[2] Fig. 12 shows typical pulse height distribution for the cathode strips measuring maximum charge in clusters (peak strip). The distribution shows Landau distribution and the typical most probable value (MPV) is 150 channel in ADC.

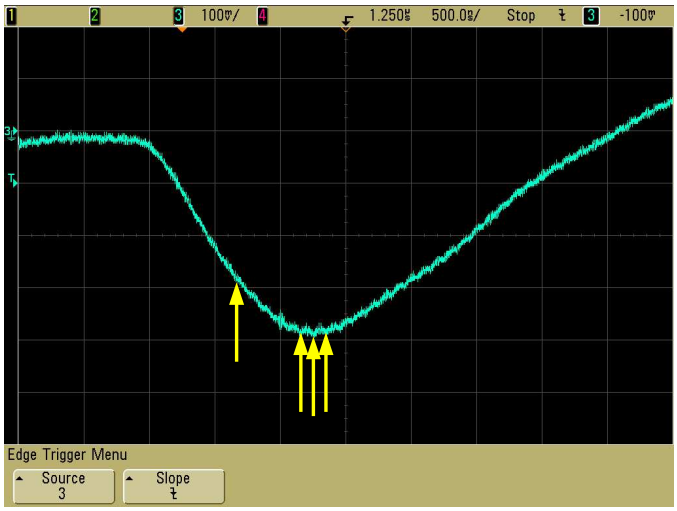



Figure 11: MuTr-FEE raw signal. The amplitudes indicated by arrows are digitized and recorded. The location of arrow is 1, 6, 7, and 8 in the unit of beam clock.

[2] Actually, current MuTr offline reconstruction code does not perform fitting but using average of latter three points for the pulse height.

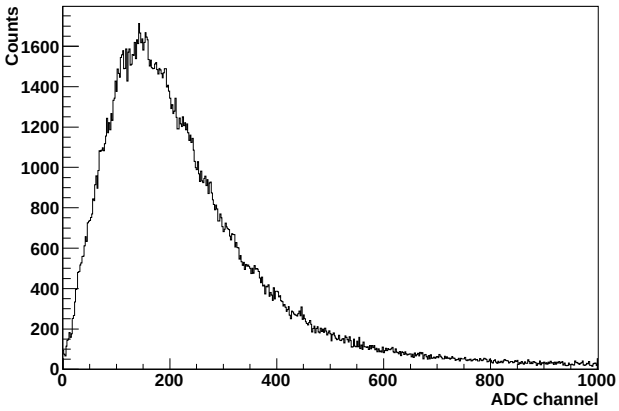



Figure 12: Typical ADC distribution of peak strips.

#### *3.1.2. Charge gain reduction*

As described in Section 2.1, MuTRG-ADTX consumes about 5 % of the signal charge. As a consequence the gain for the particle energy deposit is reduced at the input of MuTr-FEE. It causes that noise fluctuation becomes relatively larger compared to signal. We will discuss degradation of performance due to increased noise level in Section 3.1.3. Another concern is strip-dependent variety of gain reduction. Because position of particle trajectory is determined by profile of strip-by-strip charge deposit, gain non-uniformity could result in degradation of position resolution, although, in principle, such gain non-uniformity is corrected by calibration pulse. Fig. 13 shows typical pulse height reduction by MuTRG-ADTX installation and measured using calibration pulse. The gain on MuTr-FEE is reduced to be about 90 % in average. The gain reduction using cosmic ray was also measured at the test in 2007 and was 94 %. The reason of gain reduction difference between calibration pulse data and cosmic ray data is supposed to be due to frequency dependence of op-amp gain and different frequency component of calibration pulse and cosmic ray. Variety of the gain reduction over strips turns out to be less than 1 % in sigma based on Fig. 13. If the variety is considered as background noise, the corresponding noise level which is discussed in Section 3.1.3 is estimated to be much smaller than 1 %, expecting that the calibration with MuTRG-ADTX installed correct the gain reduction variety. Based on Fig. 15, this effect is sufficiently small.

#### *3.1.3. Noise level*

Installing MuTRG-ADTX is equivalent to inserting additional capacitance in view from existing MuTr-FEE. It causes increase of noise on MuTr-FEE which results in degradation of position resolution, therefore it is important to keep noise level as low as possible. Fig. 14 shows the pedestal RMS distribution on MuTr-FEE before and after installing the MuTRG-AD board. The distribution is supposed to represent the size of noise. By installing MuTRG-AD, noise increased by about 30 %. The noise increase is smaller at longer strips region be-

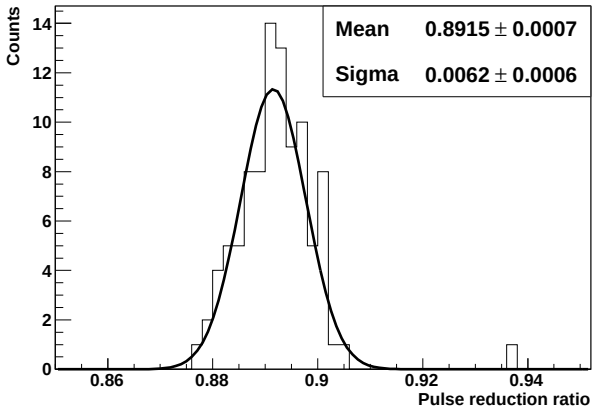



Figure 13: Pulse height reduction on MuTr-FEE by installing MuTRG-ADTX. Each entry corresponds to the measurement for a strip. Data from a certain cathode plane in Station-1 as a typical case.

cause longer strips have originally larger capacitance and relative increase of capacitance due to MuTRG-ADTX installation is small.

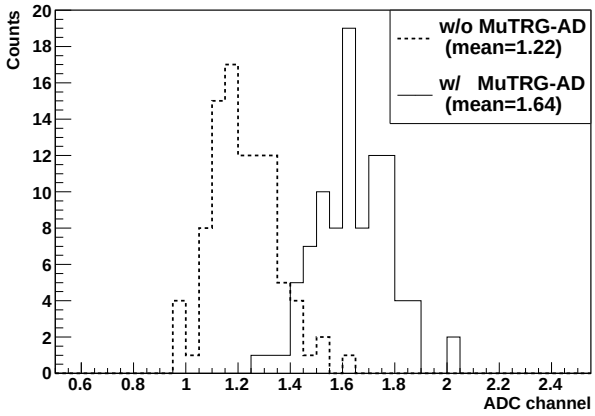



Figure 14: Distribution of the pedestal RMS on MuTr-FEE measured at the test experiment in 2007. Each entry of histograms corresponds to the measurement for a strip. The histograms with dashed line and solid line were measured before and after installing MuTRG-AD board, respectively.

Finally position resolution can be evaluated using noise to signal ratio. We name noise level as the ratio of noise divided by signal pulse height. Fig. 15 shows position resolution as a function of noise level measured in the electron beam test experiment in 2006. The impact of noise increase on the position resolution is described only by noise level and is independent from the installation of the MuTRG-AD board. Based on this results, we concluded that the degradation of the position resolution by installing MuTRG-ADTX can be evaluated using a parameter of the noise level. After installing MuTRG-ADTX boards, the noise level became about 1.1 %, which is ∼30 % increase compared to before installation. This noise level corresponds to the position resolution of about 110 $\mu$m based on Fig. 15 and we decided the noise level achieved to the sufficient value. Because the noise level is defined as the noise divided by the signal height, we can improve it by increasing signal pulse height. Raising high voltage of MuTr by 25 V on average can compensate for the 30 % increase of the noise level.

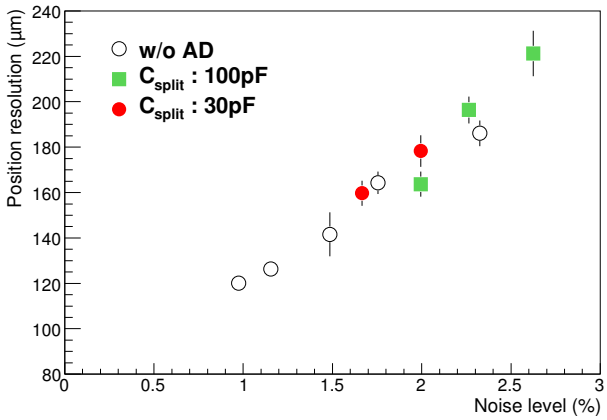



Figure 15: Position resolution as a function of noise level. The data were measured with electron test beam at Tohoku University in 2006, at which MuTRG-ADTX was separated into analog (AD) and digital (TX) part, and only the MuTRG-AD board are used in this measurements. The position resolution in the plot includes resolution of 50 um from reference detector of Silicone Strip Detector. Three data sets of without MuTRG-AD, with MuTRG-AD ($C_{split}$ = 100 pF) and with MuTRG-AD ($C_{split}$ = 30 pF) are displayed together. (The $C_{split}$ of production version is 56 pF.) No significant difference between data sets are observed.

### *3.1.4. Signal timing*

Because of small input capacitance of 56 pF in MuTRG-ADTX, higher frequency current component of the signal charge, mostly rising part, is selectively filtered and processed into MuTRG-ADTX. As a consequence, the signal peak timing on MuTr-FEE is delayed due to smeared rising. The timing distributions of the signal peak on MuTr-FEE between with and without the MuTRG-AD board installed are compared in Fig. 16. The timing shifts by about one beam clock.

Because MuTRG-ADTX was installed in only non-stereo cathode plane but the adjustment knob of the trigger timing for MuTr-FEE readout is common over all cathodes in each station, the trigger timing can not be optimized for all cathode plane. For this reason, we need to evaluate strip-by-strip gain variation due to unoptimized signal timing, though such variation can be canceled by calibration using test pulse to a certain degree. Fig. 17 shows ratio of pulse height on MuTr-FEE with artificial timing shift divided by that with optimized timing. Both the average gain shift and the strip-to-strip variation due to the signal timing shift of one beam clock are smaller than 1 % and can be ignored compared with noise on MuTr-FEE.

## *3.2. Performance of MuTRG-ADTX*

In this section, we concentrate on evaluating the performance of MuTRG-ADTX itself. MuTRG-ADTX has capability of selecting CFD or LED. In this section, the measurement was done

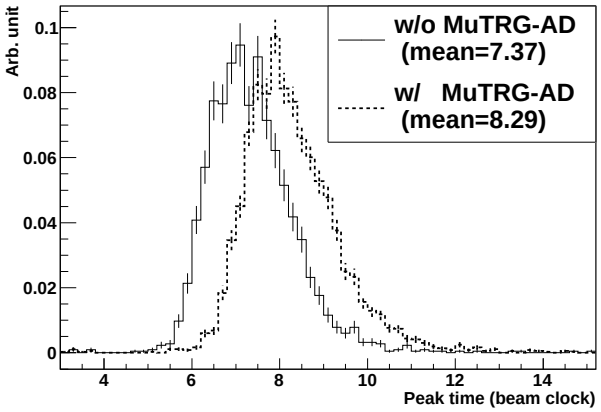



Figure 16: Timing distribution of the MuTr-FEE signal. Solid and dashed line show results of measurements with and without MuTRG-AD installed, respectively. This measurements were performed with cosmic ray in 2007.

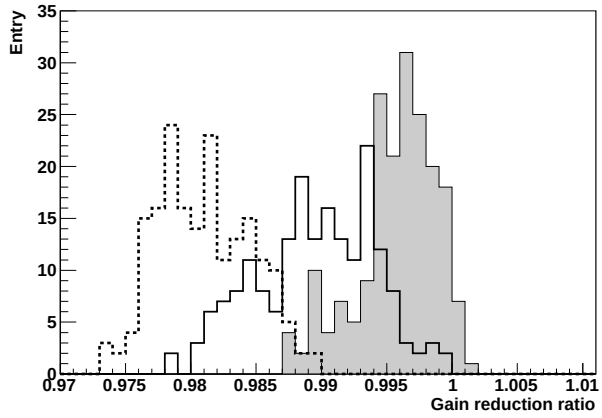



Figure 17: Ratio of signal pulse height on MuTr-FEE with artificial timing shift divided by that with optimized timing. Calibration pulse is used for the measurements. The distributions are integral of all strips in a octant. Filled histogram, unfilled histogram with solid line and unfilled histogram with dashed line were measured with 1, 2 and 3 beam clock delay, respectively.

with CFD unless otherwise noted. We will compare CFD and LED in Section 3.2.4.

### *3.2.1. Fake hit rate*

Fake hits caused by noise are preferred to be as small as possible because they can produce fake trigger due to random coincidence of 3 stations or random coincidence with beam-related background. Fig. 18 shows fake hit rate as a function of threshold for a typical single strip. The fake hit rate becomes exponentially reduced by increasing threshold. The fake hit rates are slightly higher in the region where longer strips are because the the noise are coupled to the size of the capacitance. Based on GEANT simulation, it turns out that the trigger rejection power is kept for the random fake hit rate up to 100 kHz.

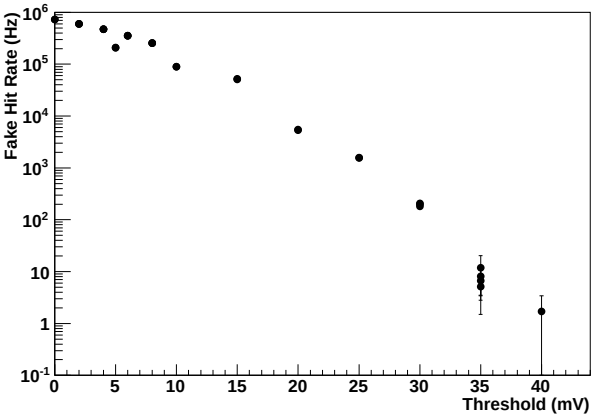



Figure 18: Fake hit rate as a function of threshold for a typical strip. Measurement was performed with beam test at PHENIX in 2008.

### *3.2.2. Efficiency of each cathode plane*

Important performance of MuTRG-ADTX is efficiency because its degradation directly causes inefficiency of the trigger. Fig. 19 shows efficiency turn-on curve for single cathode plane as a function of ADC measured by MuTr-FEE readout. Peak strips of clusters are picked up for the calculation. The efficiencies at plateau achieved to be more than 90 % and the turn-on point is typically 60 channel in ADC when threshold of 30 mV is applied. The major source of the inefficiency at the plateau is timing cut of three beam clocks. Comparing to MPV of ~150 channel in ADC distribution, the turn-on point is sufficiently small. Overall efficiency for the ADC distribution of the peak strip is about 90 %. Because MuTRG-ADTX was installed in three planes for Station-1, and two planes for Station-2 and 3, the efficiency is expected to be more than 99 % when we require OR of planes. When we require hits in two planes out of three planes for Station-1, the efficiency is expected to be more than 97 %.

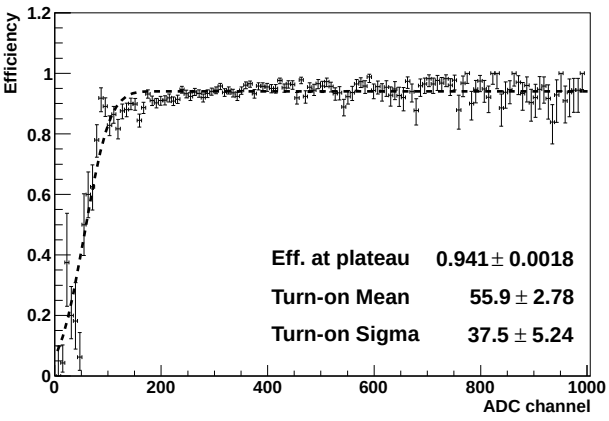



Figure 19: Typical efficiency of MuTRG-ADTX for a single cathode plane as a function of ADC measured by MuTr-FEE. Threshold of 30 mV was applied.

### 3.2.3. Signal timing

Fig. 20 shows timing distribution of MuTRG measured with cosmic ray as well as beam collisions at RHIC. The results from cosmic ray data and beam data are consistent with each other. MuTRG alone can not determine a beam crossing at which collision occurs because the timing resolution is over the interval of the beam crossings of 106 nsec. MuTRG system works as trigger by making AND with other trigger with good timing resolution. BBC at low luminosity condition or RPC can provide the trigger timing.

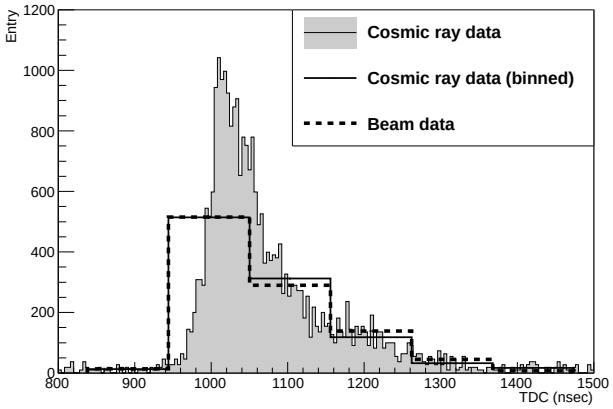



Figure 20: The signal timing of MuTRG-FEE measured with cosmic ray as well as beam. CFD is adopted in these measurements. The histogram with solid line and filled with gray color was obtained in the cosmic ray measurements in 2007. The unfilled histogram with solid line is obtained by binning the original histogram of cosmic ray data with width of the beam clock of 106 nsec. The histogram with dashed line was obtained in the beam test at PHENIX in 2009. The binning for the histogram of cosmic ray data is performed to be the best match with the beam data.

Depending on the timing resolution, the timing acceptance window has to be open widely to achieve high efficiency. On the other hand, wider window would increase probability of the fake trigger due to accidental coincidence. Based on Fig. 20, the efficiency for a single hit of MuTRG achieve to 93 % at plateau in case of the timing window of three beam clocks, which we applied in the 2011 RHIC Run. It's to be noted that the efficiency becomes more than 99 % by taking OR of multiple cathode planes. The resulting performance of MuTRG-FEE in the 2011 RHIC Run is shown in Section 5.

To maximize efficiency with given width of the timing acceptance window, fine tuning of the location of the window can be performed. However, because the location of the window is synchronized with the beam clock, its optimization also causes shift of the beam clock phase in MuTRG-ADTX. For this reason, the phase can not be optional freely, but there are timing constraint between MuTRG-ADTX and downstream electronics such as MuTRG-MRG and LL1 module. The beam clock phase for MuTRG-ADTX is optimized satisfying the constraint.

### 3.2.4. Performance difference of CFD and LED

We adopted LED instead of CFD in the measurement at the 2011 RHIC Run because the faster trigger timing is preferable to install MuTRG to the PHENIX trigger system. We evaluate the performance difference between CFD and LED in this section. The demerits of LED are time walk effect and degradation of timing resolution. Fig. 21 shows MuTRG hit timing as a function of ADC. The time walk effect of about one beam clock is observed in the measurement with LED. The RMS of the hit timing is about one beam clock and is better in CFD by ~0.1 beam clock than LED. When we applied three beam clock acceptance window for the trigger, the degradation of the efficiency in LED is a few % compared to CFD.

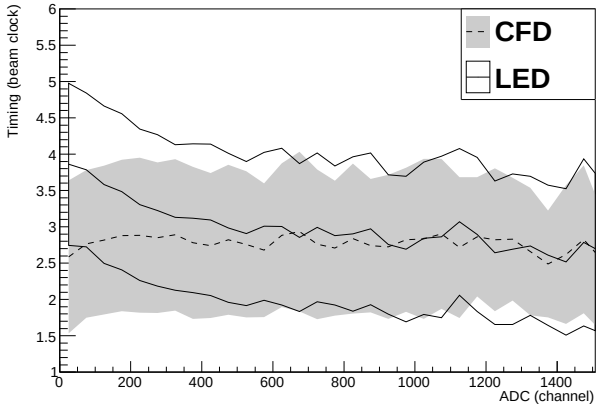



Figure 21: Pulse height dependence of the hit timing of MuTRG-FEE. ADC is measured by MuTr-FEE. The time zero of the vertical axis is arbitrary, but offset of three beam clocks is added between two data sets. The center line and the band indicate mean value and RMS of the timing distribution, respectively.

## 4. MuTRG-MRG board and MuTRG-DCMIF board

A snapshot of the strip hits at each beam clock tick is taken and transferred to the data merger board (MuTRG-MRG, Fig. 22). The MuTRG-MRG board receives data from the MuTRG-ADTX boards at a rate of 1.2 Gbps. After merging and reformatting data from multiple MuTRG-ADTX boards, the MuTRG-MRG board sends hit data, sorted by strip number, to the LL1 module at a rate of 2.8 Gbps for the Level-1 trigger decision.

The MuTRG-MRG also sends data to the DCM through an interface board (MuTRG-DCMIF, Fig. 27) upon a Level-1 trigger accept signal from the PHENIX granule timing module (GTM).[7]. The MuTRG-DCMIF board combines triggered data from eight MuTRG-MRG boards, and sends them to the DCM. The data recorded by the DCM is to be used to monitor and diagnose the trigger electronics in online/offline analyses.

The beam clock and other control signals from the GTM are received by the MuTRG-DCMIF board. The MuTRG-DCMIF board distributes the control signals (beam clock, Level-1 trigger accept, mode bits) to MuTRG-MRG boards. The MuTRG-

MRG boards then distributes the control signals (mode bits) to MuTRG-ADTX boards.

The MuTRG-MRG and MuTRG-DCMIF boards have an interface with the VME bus (A24D16) through the VME J1 backplane. Seven bits in the VME address space are used to identify the board in the VME bus. Another seventeen address bits are used to address internal registers in MuTRG-MRG and MuTRG-DCMIF boards. Slow control signals to MuTRG-MRG and MuTRG-DCMIF boards are passed through the VME bus by writing onto internal registers. The slow control signals are provided to the MuTRG-ADTX board with a 1.2 Gbps serial link. The MuTRG-MRG board is used to interface the VME bus to the serial link for the slow-control of the MuTRG-ADTX boards.

The MuTRG-MRG and MuTRG-DCMIF boards are installed in 9U VME sub-racks in the rack room. Two VME sub-racks are used to cover each muon arm. Each VME sub-rack accommodates sixteen MuTRG-MRG boards and two MuTRG-DCMIF boards. The VME sub-rack is controlled by the single board computer board (MVME2300). Hardware specifications of MuTRG-MRG and DCMIF boards are given in Table 4. Detail of the MuTRG-MRG and MuTRG-DCMIF boards are described in following sections.

### *4.1. MuTRG-MRG board*

#### *4.1.1. Design*

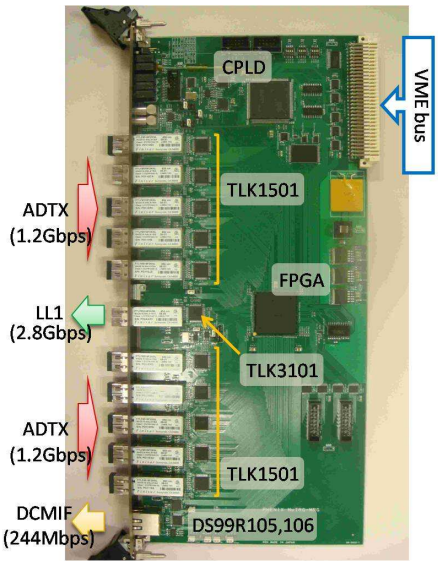



Figure 22: MuTRG-MRG board

MuTRG-MRG is a module to transmit hit patterns from MuTRG-ADTX to LL1 module and MuTRG-DCMIF. Fig. 22 shows MuTRG-MRG board. Main roles of MuTRG-MRG are the following.

- Receives the data from MuTRG-ADTX and extracts hit patterns from them.
- Transmits the extracted hit patterns to LL1 module to generate Level-1 trigger signals for high-momentum tracks.
- Transmits the identical hit patterns as which are sent to LL1 module to PHENIX main data stream as well via MuTRG-DCMIF for offline analysis.
- Controls MuTRG-ADTX boards remotely.

In order to satisfy the capability of multiple functions required as above, a FPGA (XC3S4000_5FG900C, Xilinx) was employed. Detail design of the FPGA is mentioned in Section 4.1.2.

As Fig. 22 shows, MuTRG-MRG has following I/O channels.

- 10 optical transceiver channels for connection with MuTRG-ADTX.
- An optical transceiver channel for connection with LL1 module.
- A modular connector for connection with MuTRG-DCMIF.
- A connector for connection with VME bus.

On the top of the front panel, 9 LEDs are implemented as error indicators for diagnoses of some common failures. MuTRG-MRG can be controlled through VME64x. MuTRG-MRG requires 3.3 V power input. The power line generates about 4.3 A of current in normal operation. The dimensions of MuTRG-MRG is 9U (400 mm) in height, 160 mm in depth and 1.6 mm in thickness. The 9U height is determined to meet a spatial requirement for the I/O channels on the front panel of MuTRG-MRG. The FPGA has 712 I/O pins (ball-grid-array, BGA package) and most of them are in use. The circuit board is composed of 10 layers because of a requirement of the connections of electronic wires with the many I/O channels on FPGA.

Since MuTRG-MRG has high speed signal lines, the layout of chips and modules and the signal wiring on MuTRG-MRG are to be concerned. High speed lines on MuTRG-MRG are 2.8 Gbps serial signal lines, between TLK3101 (Texas Instruments) and an optical driver for the transmission to LL1 module, and 140 MHz 18-bit parallel lines, between FPGA and TLK3101. Even little impedance mismatching in these lines causes distortions of the signals. Also ringing due to incorrect termination should be minimized since rising times of the signals are very fast. Taking into account these concerns, the FPGA, the TLK3101 and the optical driver are arranged as close to each other as possible as Fig. 22 shows, and all edges in corners of the rapid signal lines are made smooth for the impedance matching.

#### *4.1.2. Data handling and data format*

MuTRG-MRG produces a 192-bit hit pattern from the MuTRG-ADTX data as Fig. 23 shows. MuTRG-MRG receives the data coming from MuTRG-ADTX boards by using transceiver chips, TLK1501. Each TLK1501 receives serial data at an effective serial rate of 1.2 Gbps, providing 960 Mbps of data bandwidth, and decodes it to 16-bit parallel data at a rate of 60 MHz. These parallel data include information of hit patterns of MuTr and event counter values that

Table 4: Specifications of MuTRG-MRG and MuTRG-DCMIF

| MuTRG-MRG | |
|---|---|
| Number of modules | 64 (32 per arm) |
| I/O | 10 (1.2 Gpbs optical link to MuTRG-ADTX) |
| | 1 (2.8 Gpbs optical link to LL1 board) |
| | 1 (0.2 Gpbs serial link to MuTRG-DCMIF) |
| Size | VME 9U (160 mm depth) |
| Voltage | +3.3 V |
| Power consumption | ~4.3 A (in normal operation) |
| **MuTRG-DCMIF** | |
| Number of modules | 8 (4 per arm) |
| I/O | 8 (1.2 Gpbs optical link to MuTRG-MRG) |
| | 1 (1.6 Gpbs serial link to DCM) |
| | 1 (0.2 Gpbs optical link to GTM) |
| Size | VME 9U (160 mm depth) |
| Voltage | +3.3 V, +5.0 V |
| Power consumption | ~1.2 A(+3.3 V), ~0.5 A(+5.0 V) |

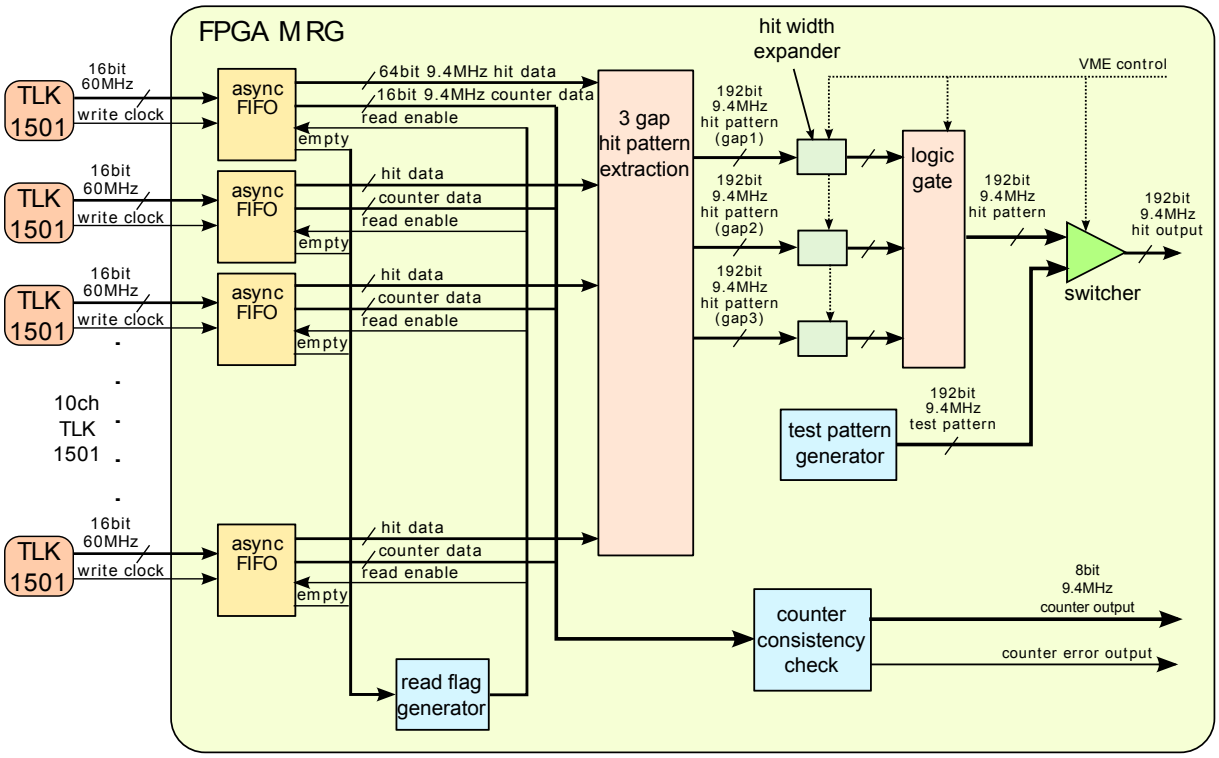



Figure 23: Block diagram of data flow in MuTRG-MRG board from transceiver chips (TLK1501), which receive MuTRG-ADTX data, to completion of hit data extraction. The first asynchronous FIFO synchronize the data with beam collision frequency (9.4 MHz).

inform the MuTRG-MRG board from which collision the event comes. These counter values are adjusted by a simultaneous reset of MuTRG-ADTX so that all data from a same collision are tagged by an identical event counter value. Fig. 23 shows a block diagram of hit pattern extraction in MuTRG-MRG. Parallel data from all MuTRG-ADTX boards are sent to FPGA. They are not synchronized because each MuTRG-ADTX uses an independent internal clock for the data transmission. Therefore the FPGA synchronizes all the data from MuTRG-ADTX as follows. When reset signals for MuTRG-ADTX are released and the first data from these boards reach to the FPGA on MuTRG-MRG, memories of all first-in-first-out (FIFO) are empty and not read yet. The readouts of the FIFO memories starts simultaneously right after the all first data are written on the memories. Then the outputs of the memories are completely synchronized by a read clock with a RHIC beam

clock of 9.4 MHz.

The MuTRG-ADTX boards are installed in three planes of MuTr for Station-1, and two planes for Station-2 and 3. The hit patterns of three or two MuTr planes are extracted from the synchronized data in the FPGA. MuTRG-MRG merges the data from multiple cathode planes by taking OR/AND for strips which cover same acceptance. This merging scheme is optional and can be controlled through VME to optimize the efficiency and the fake hit rate. For Station-1, intermediate setting of AND2 which requires two hits out of three planes can be selected. MuTRG-MRG can also force any channels to fire and the function is useful to diagnose a source of problems in the operation.

MuTRG-MRG transmits the merged hit pattern to LL1 module. Fig. 24 shows the diagram of the transmission. MuTRG-MRG converts the hit pattern into an array of 16-bit data packets and adds a counter packet including a counter value, an ID number of the MuTRG-MRG board and an error bit, on the front of the array as a header. The array of the packets are sent and written to asynchronous FIFO at a rate of 9.4×14 MHz and read with 140 MHz oscillator clock. The data read out from the FIFO are sent to a transceiver chip, TLK3101 (Texas Instruments), toward the LL1 module. The TLK3101 encodes the data into a serial signal at an effective serial rate of 2.8 Gbps, providing 2.24 Gbps of data bandwidth. The encoded signal are transmitted to the LL1 module via an optical driver. As a consequence of above processes, MuTRG-MRG requires 230 – 300 nsec data-processing time between the output of TLK1501 and the input of TLK3101.

When MuTRG-MRG receives a PHENIX Level-1 trigger, MuTRG-MRG transmits hit patterns associated with the collision that generated the trigger to MuTRG-DCMIF which transmits the data to DCM. Fig. 25(a) shows scheme of the transmission to MuTRG-DCMIF. After MuTRG-MRG transmits a hit pattern to the LL1 module, MuTRG-MRG has to wait for about 3 $\mu$sec until Level-1 trigger decision will be performed and the trigger accept signal will arrive at MuTRG-MRG. Therefore MuTRG-MRG has a function to memorizes the hit pattern in every collision for 13 $\mu$sec utilizing a shift register. At the Level-1 trigger reception, MuTRG-MRG recalls a hit pattern on a corresponding depth of the shift register. This depth is called "latency" and should be fixed during data taking. The latency can be adjusted with VME access so that the recalled pattern is correctly associated with the collision which generated the Level-1 trigger.

It is technically difficult to transmit all hit data associated with a trigger to the downstream MuTRG-DCMIF within 106 nsec interval of the beam clock cycle. Therefore, multiple event buffers are employed on MuTRG-MRG. The number of the buffers is eight so that up to consecutive eight Level-1 triggers can be handled with the buffers. Because current PHENIX DAQ has up to five event buffers and it means the maximum number of consecutive triggers coming to MuTRG-MRG is five, the eight event buffers in MuTRG-MRG are enough size to process the data in the PHENIX data taking system. Inner structure of each event buffer is shown in Fig. 25(b). To evaluate performance of MuTRG-FEE in offline analysis, MuTRG-MRG transmits hit patterns for several beam clocks around an event associated with the trigger to MuTRG-DCMIF. The size of the tolerance window of the transmitted data can be set to a range from 1 to 7 beam clocks through VME. As Fig. 25(b) shows, an event buffer in Fig. 25(a) has $n$ event registers to store the hit patterns of consecutive $n$ collisions, where $n$ (=1 – 7) represents the number of the beam clocks of the window. Two multiplexers converts these hit patterns into an array of 16-bit data packets at a rate of 9.4 MHz. These data packets are written to FIFO.

At last, MuTRG-MRG adds 8-bit information data such as data number, data type flag and error flag to these 16-bit data packets to reformat them to 24-bit data packet array. After adding a packet of the trigger counter value as a header, the data packet array is sent to a transmitter chip, DS99R105 (National Semiconductor), at a rate of 9.4 MHz. They are encoded into a serial signal with an effective serial rate of 244 Mbps, providing 226 Mbps of data bandwidth. The signals are sent to MuTRG-DCMIF through a category-6 Ethernet cable.

*4.1.3. Control signals for MuTRG-MRG and MuTRG-ADTX*

MuTRG-MRG requires various kinds of control signals from MuTRG-DCMIF and VME-bus. The required signals are following.

- Reset of registers ... (**MuTRG-DCMIF**+**VME**)
- Reset for a phase-locked loop (PLL) on FPGA ... (**MuTRG-DCMIF**+**VME**)
- Commands for MuTRG-ADTX control (DAQ start, reset, running mode setting) ... (**MuTRG-DCMIF**+**VME**)
- Trigger signal ... (**MuTRG-DCMIF**)
- Configuration signal for FPGA and PROM on MuTRG-MRG ... (**VME**)
- Setting of the latency value[3] ... (**VME**)
- Setting of the required number of hits (OR/AND) in MuTr cathode planes ... (**VME**)
- Commands for MuTRG-ADTX setting (threshold, FPGA and PROM configuration) ... (**VME**)

These control signals are sent from MuTRG-DCMIF and VME. The contents in the parentheses at the end of each sentence shows which module sends the signal to MuTRG-MRG. A 9.4 MHz beam clock signal, which is essential for MuTRG-MRG data process, is also distributed from MuTRG-DCMIF.

As MuTRG-DCMIF controls MuTRG-MRG, MuTRG-MRG also controls MuTRG-ADTX. Since it is not easy to access physically to the volume of MuTr where MuTRG-ADTX are installed, this remote control system for MuTRG-ADTX is as important as the data process for the MuTRG-FEE system. MuTRG-MRG has following control functions for MuTRG-ADTX.

[3] The meaning of the latency is mentioned in Section 4.1.2.

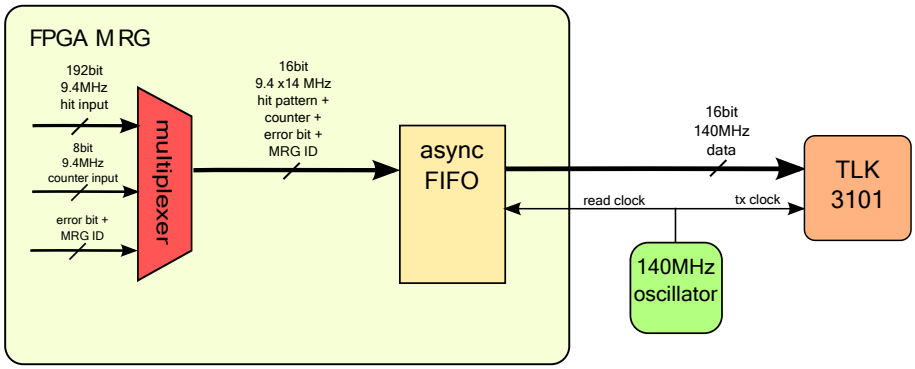



Figure 24: Block diagram of data flow of extracted 192-bit hit pattern in MuTRG-MRG board to a transceiver chip (TLK3101), which encodes the pattern to a 2.8 Gbps serial signal.

- Start of the data transmission
- Reset of registers
- Reset for a phase-locked loop (PLL) on FPGA
- Setting of threshold voltages for the hit decisions
- CFD and LED mode selection
- Configuration signal of FPGA and PROM
- Acquisition of a board ID number

MuTRG-MRG sends these control signals to MuTRG-ADTX with transceiver chips, TLK1501.

*4.1.4. Error handling*

If some errors happen on MuTRG-MRG, MuTRG-MRG indicates the errors with 9 LEDs on the front panel. MuTRG-MRG also sends error signals to LL1 module and MuTRG-DCMIF. The errors are memorized on registers in FPGA and can be read through VME readout bus. Fig. 26 shows a picture of the status indicators and table 5 shows corresponding symptoms. These indicators help to diagnose any problems on MuTRG-MRG. Some important parts of the error information are sent to DCM through MuTRG-DCMIF together with hit data.

*4.2. MuTRG-DCMIF board*

*4.2.1. Design*

MuTRG-DCMIF is an essential board to transmit hit patterns to DCM at trigger reception for data collection. Fig. 27 shows a picture of the MuTRG-DCMIF board. MuTRG-DCMIF has following main roles.

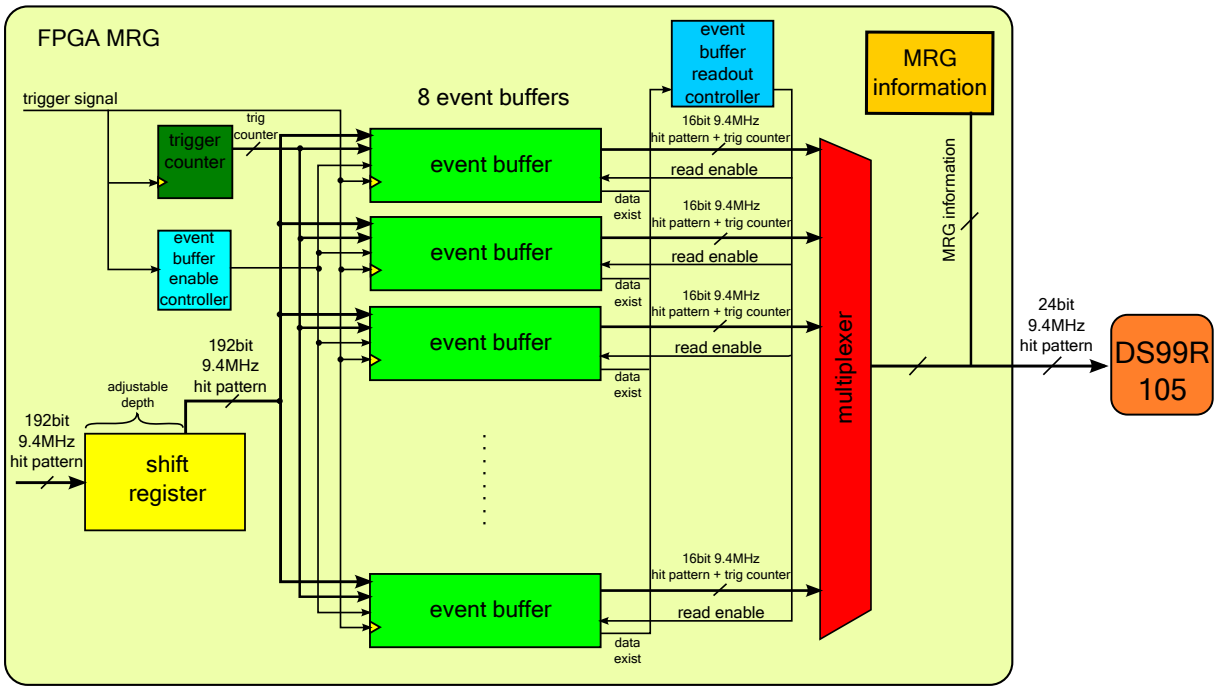
- To transmit hit patterns at trigger decision to DCM to record the hit patterns.
- To distribute timing signals to MuTRG-MRG, for example the beam clock, a trigger signal and several kinds of control signals for MuTRG-MRG and MuTRG-ADTX.


Figure 26: Status indicators on the front panel of MuTRG-MRG. The top 6 LEDs are for power monitoring. The middle 9 LEDs are error indicators. Table 5 shows symptoms these LEDs indicate.

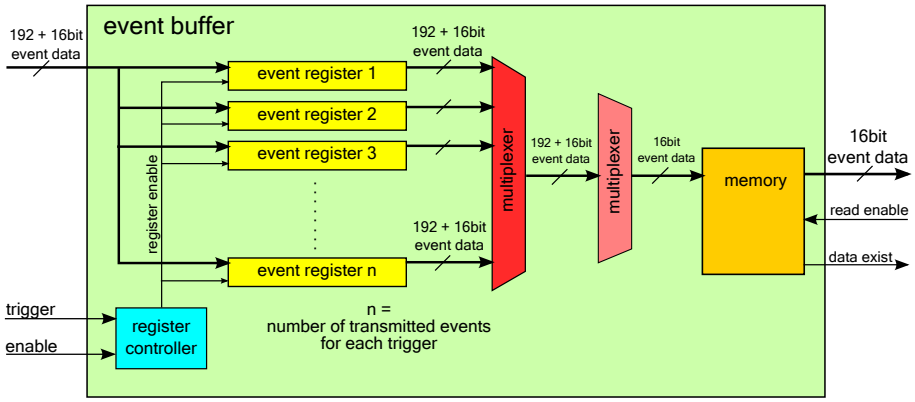
Table 5: Symptoms corresponding to LEDs shown in Fig. 26

| **LED #** | symptom |
|---|---|
| **LED 0** | ADTX-MRG link error |
| **LED 1** | error propagation from ADTX |
| **LED 2** | clock counter inconsistency |
| **LED 3** | FIFO full error |
| **LED 4** | FIFO (ADTX interface) unexpected empty |
| **LED 5** | FIFO (DCMIF interface) unexpected empty |
| **LED 6** | no process running |
| **LED 7** | Digital Clock Manager unlock |
| **LOCK** | MRG-DCMIF link error |

As well as MuTRG-MRG, MuTRG-DCMIF merges many input data. In this point of view, the basic concept of MuTRG-




(a) data flow diagram for data transmission to MuTRG-DCMIF in MuTRG-MRG




(b) data flow diagram in each event buffer

Figure 25: (a) Block diagram of transmission of extracted 192-bit hit pattern in MuTRG-MRG board to a transmitter chip (DS99R105), which transmits the data to MuTRG-DCMIF. (b) Block diagram of the event buffer in the figure (a).

DCMIF design is same as MuTRG-MRG. The same FPGA as MuTRG-MRG, namely XC3S4000_5FG900C (Xilinx), is employed on MuTRG-DCMIF. MuTRG-DCMIF is controlled through VME64x. MuTRG-DCMIF requires 3.3 V and 5.0 V power input. The 3.3 V and 5.0 V power lines generate about 1.2 A and 0.5 A of current respectively. Dimension of MuTRG-DCMIF is 9U (400 mm) $\times$ 160 mm $\times$ 1.6 mm. The dimension is optimized by the spatial requirement of the front panel and the production cost. The circuit board composed of 10 layers because of the connection between signal wires and many I/O channels on FPGA. MuTRG-DCMIF has following I/O channels.

- 8 modular connectors for connection with MuTRG-MRG.
- An optical transmitter channel for connection with DCM.
- An optical receiver channel for connection with GTM.
- A connector for connection with VME bus.

*4.2.2. Data format*

As mentioned in the previous section, MuTRG-MRG sends a serial signal including hit pattern information and a trigger

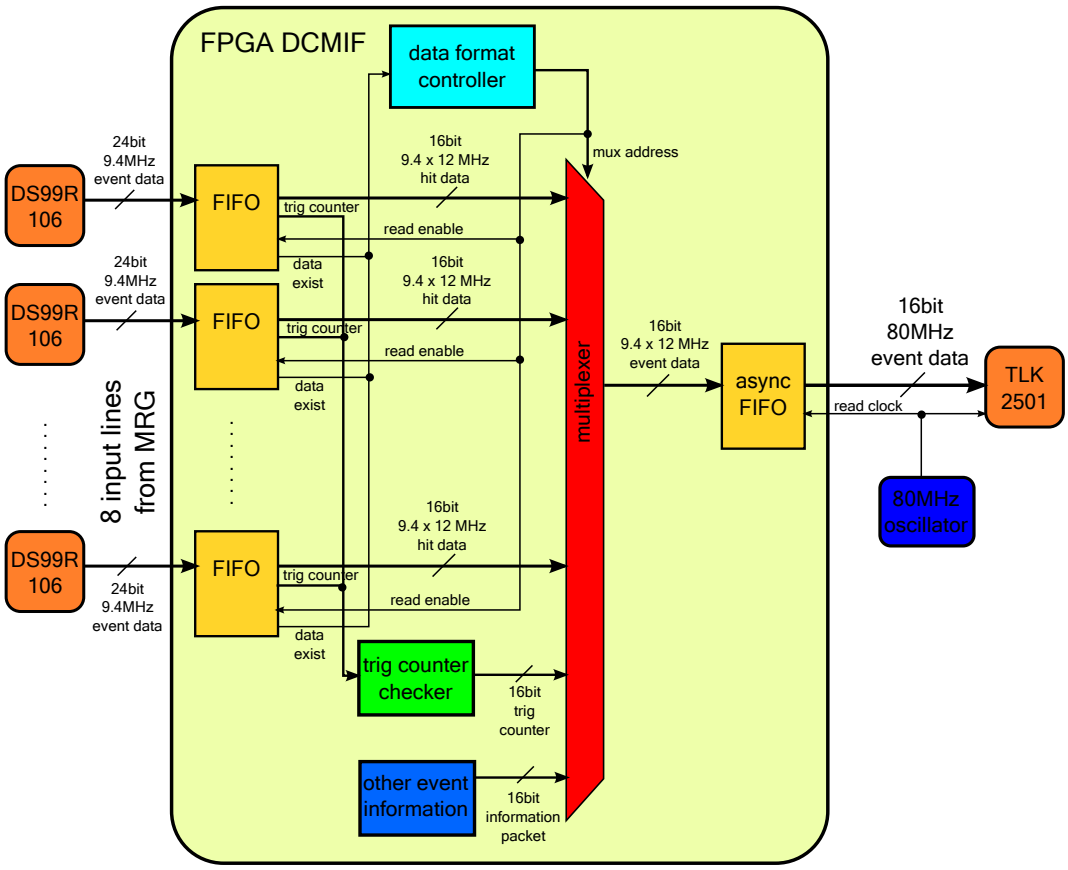



Figure 28: Block diagram of data flow in MuTRG-DCMIF board.

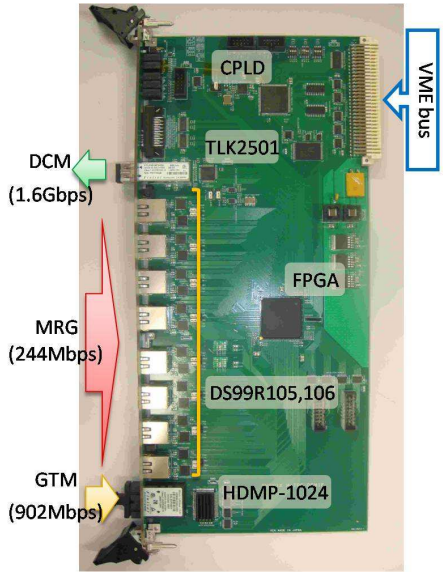



Figure 27: the MuTRG-DCMIF board

counter value with an effective rate of 244 MHz. MuTRG-DCMIF receives the serial signals from eight MuTRG-MRG boards, which correspond to the hit information for two octants of MuTr, by using eight receiver chips, DS99R106 (National Semiconductor). The eight DS99R106 decode the signals into arrays of 24-bit data packets at a rate of 9.4 MHz. The arrays are same as those before the encoding on MuTRG-MRG by DS99R105. These decoded data arrays are sent to FPGA on MuTRG-DCMIF, in which these packets are written to FIFO memories. After a readout controller confirms that all FIFO have valid data, readout of the written data starts. In the read process, a multiplexer aligns output data packets in a fixed format explained in the following.

At first, 16-bit trigger counter values are read from all FIFO and compared with each other in FPGA to confirm their consistency. If inconsistency is found in the values, an error flag is issued. The multiplexer transmits the trigger counter value as the first packet of output data. Following the trigger counter packet, the multiplexer consecutively sends other four header packets including additional event and module information. The header packets consist of following information.

- A trigger counter packet, which counts an event number.
- A flag packet, which is not used in this system and fixed to 0xffff. It's reserved for a future use.
- A detector ID packet, which notifies whether the data comes from the North arm or the South arm.

- A module address packet, which indicates an ID number of the MuTRG-DCMIF board.
- A clock counter, which indicates a beam-clock counter value at the trigger reception.

After these header packets, the multiplexer reads hit data packets from the FIFO with changing their order according to a suitable format. The size of the data for each event becomes 2 octants × ( 96 strips for Station-1 + 192 strips for Station-2 + 320 strips for Station-3 ) = 76 packets, where 1 packet = 16-bit.

At last, following trailers are added on the hit data packets to complete making an output data array.

- Error packets, which indicate error flags on MuTRG-MRG and MuTRG-DCMIF.
- Longitudinal parity packet, which indicates longitudinal parity of all the packets in the event data. This value is compared in DCM to confirm successful transmission.

As a result, the number of packets in the array for single trigger is 5 (header) + 76 ×$n$ (data) + 2 (trailer), where $n$ is the size of the beam clock window for which events are transmitted.

Each data packet of the array is written to latter asynchronous FIFO at a rate of 9.4 × 12 MHz. The written packets are read with 80 MHz oscillator clock and sent to a transmitter, TLK2501(Texas Instruments). The TLK2501 encodes the 16-bit data packets into a serial signal with an effective serial rate of 1.6 Gbps, providing 1.28 Gbps of data bandwidth. The serial signal are sent to DCM via an optical driver.

#### *4.2.3. Control signals for MuTRG-DCMIF*

Timing control signals for MuTRG-FEE system is originally generated by GTM. A serial signal from GTM is decoded with a deserializer chip, HDMP1024 (Hewlett Packard), into a collection of control signals. Main signals used in MuTRG-FEE system are the beam-clock signal, trigger accept signal and several mode bit signals. The mode bit signals are translated into reset signals for MuTRG-DCMIF, MuTRG-MRG and MuTRG-ADTX on the FPGA. These signals are distributed to MuTRG-MRG through category-6 Ethernet cables.

As well as MuTRG-MRG, MuTRG-DCMIF is also controlled through VME bus. The control signals through VME bus play following roles.

- Reset for registers
- Reset for a phase-locked loop (PLL)
- Configuration of FPGA and CPLD on MuTRG-DCMIF
- Setting of the number of transmitted events for each trigger

## 5. Muon Trigger Performance

### *5.1. Trigger logic*

Fig. 29 schematically displays the concept of the high-momentum muon trigger. The trigger is generated based on hits from each channel of MuTRG-ADTX. The basic idea to select high-momentum muons is to find a straight trajectory originated in the collision point from the hits from MuTRG-ADTX. There are several parameters to optimize the trigger performance and they are summarized below. The order of the items corresponds to actual order of the operation. Detailed explanation is provided in the following sections.

1 Threshold for the pulse height. To be balanced between the level of noise and signal pulse height. See Section 3.2.1 and 3.2.2.

2 CFD or LED. See Section 3.2.4

3 Timing window (LL1 width). See Section 5.1.1.

4 OR/AND of hits in multiple cathode planes in the same station. See Section 5.1.2.

5 Clustering on/off. See Section 5.1.3.

6 Trigger map (acceptance window and sagitta). See Section 5.1.4.

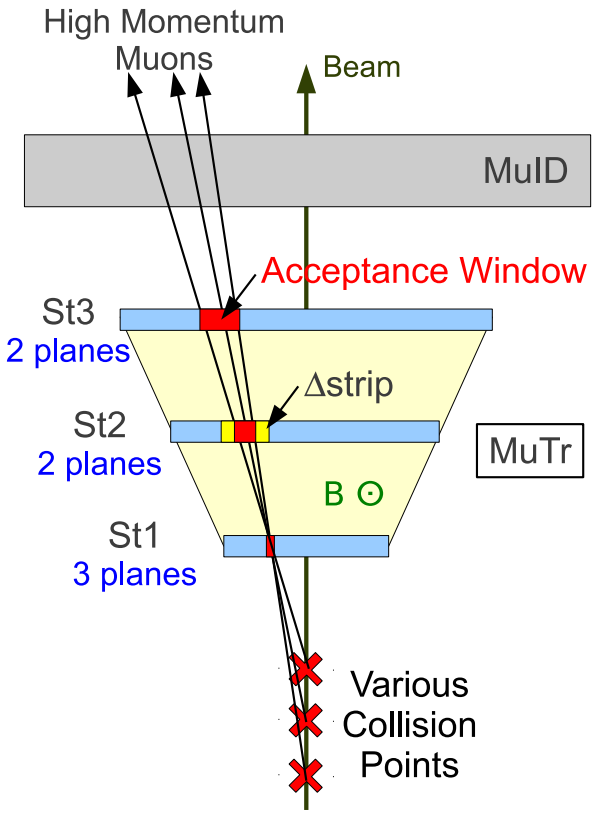



Figure 29: Explanatory drawing for the trigger logic.

#### *5.1.1. Timing window (LL1 width)*

As described in Section 3.2.3, because the timing resolution spreads over two to three beam clocks, we open up the timing window to accommodate this in the MuTRG-MRG board.

Technically, if we set the timing window to three for example, MuTRG-MRG generates artificial signal for two beam clocks following the original signal. Therefore, the output of single MuTRG-ADTX signal becomes consecutive three-beam-clock signals. Finally only one beam clock which corresponds to real collision time is selected by making AND with other timing-sensitive detector like BBC or RPC. This procedure is executed before taking signal OR/AND of multiple MuTr planes, clustering, and comparison with the trigger map.

*5.1.2. OR/AND of hits in multiple cathode planes*

MuTRG-ADTX is installed in three planes for Station 1, and two planes for Station-2 and 3. Because structure of each non-stereo planes are identical, which means corresponding strips in different gaps have the same rapidity and radial coverage, Either OR or AND mode of corresponding strip hits in multiple cathode planes can be selected. OR mode helps to enhance the trigger efficiency but is transparent against noise, while AND mode rejects fake hits, at the cost of efficiency. For Station-1, we have intermediate setting of AND2; requiring two hits out of three planes. This function is implemented in FPGA on MuTRG-MRG. See also Section 3.2.2 regarding the efficiency.

*5.1.3. Clustering*

Charge deposit by particle penetration on MuTr is shared by consecutive multiple strips (typically a few strips). This group of strips is called cluster. Compared to single strip hit, the cluster hits cause expansion of the acceptance window which results in degradation of the rejection power of the trigger. In order to minimize the defect of the cluster, an approximate center-strip finding algorithm in a given cluster, namely "clustering algorithm", was implemented in the LL1 module. The examples of the actual clustering are shown in Fig. 30. The detailed method of the algorithm is described below.

**Step 1** If successive hits are found, clustering starts.

**Step 2-1** If number of the successive hits is less than or equal to four, only the center hit is kept while other hits are discarded (Fig. 30-(a)). If number of hits in the group is two or four, only one hit with smaller channel (arbitrary) near the center is kept (Fig. 30-(b)).

**Step 2-2** Due to limited capacity of FPGA on the LL1 board, if number of the successive hits is more than four, the hits are divided into groups with less than or equal to four. Then, the same procedure of Step 2-1 is performed to each of divided sub-groups. (Fig. 30-(c))

This clustering process is carried out for each beam clock tick, after opening timing window as mentioned in Section 5.1.1. It's to be noted that this clustering algorithm also behaves like the hit multiplicity cut, although it is not implemented in this trigger system because of the limited FPGA capacity. Events with many particles which are not supposed to be $W$-production events, as well as fake triggers due to possible common noise, are suppressed by the hit multiplicity cut. Note the clustering is also costs the efficiency as described in Section 5.3 (See Table 6).

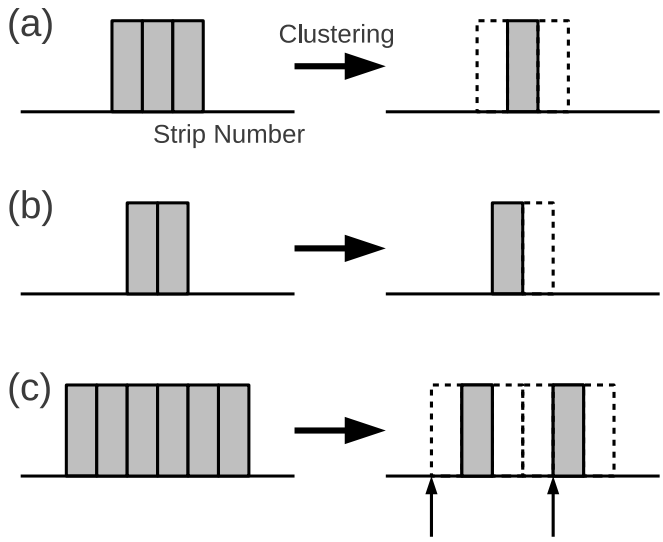



Figure 30: Three explanatory drawings for the clustering. The left side shows original hit profile and the right side is the result of the clustering. The discarded hits are indicated as the empty boxes.

*5.1.4. Trigger map*

Finally, after clustering algorithm finished, the trigger decision is made by comparing real hits and the trigger map in the LL1 module. The trigger map consists of the list of possible strip combinations of three stations which line up in a straight line as an indication of a high-momentum track. In reality, taking into account the variation of the collision point as well as multiple scattering in the material between the collision point and MuTr, the map includes combinations which satisfy a finite acceptance window as illustrated in Fig. 29. The additional acceptance window may be introduced to the map to allow not only a straight line but also small curvature of the trajectory. The latter window controls the momentum threshold of the trigger and is determined by deviation from the interception at Station-2 of the linear interpolation between Station-1 and 3. The deviation is represented in the unit of number of strips and called $\Delta$strip. For example, $|\Delta\text{strip}| \leq 1$ means that we allow three strips around the straight trajectory. Finally, the combinations of hits which are allowable for triggering are extracted based on GEANT simulation and the map is programed in the LL1 module to function as a look-up table.

*5.2. MuTRG operation in the 2011 RHIC Run*

MuTRG-FEE was installed in the RHIC shutdown period of 2008 and 2009. The first physics data were taken from the operation in the 2011 RHIC Run of polarized proton-proton run. The operating condition is listed below.

- Threshold for analog signals which is common over all channels in each MuTRG-MRG and optimized to achieve more than 97 % station efficiency at plateau. Average threshold is 25 mV.
- LED as the discriminator method. We adopt faster trigger timing to adjust to the PHENIX trigger system.

- AND2 for Station-1. OR for Station-2 and 3.
- Timing window of three beam clocks.
- Do clustering.
- $|\Delta\text{strip}| \leq 1$ in the trigger map.

In addition to MuTRG-FEE, we utilized MuID and BBC trigger[11] instead of RPC for the physics trigger in the 2011 RHIC Run. The observed performance of the MuTRG-FEE is discussed in the following sections.

### *5.3. Efficiency for track*

As explained in Section 5.1.4, the trigger decision is made by comparing hits of MuTRG-FEE and the trigger map online. To evaluate the MuTRG-FEE efficiency for a given track extracted by MuTr-FEE, the emulation of the trigger decision is performed in the offline analysis using MuTRG-FEE hits recorded into the PHENIX data stream. Any fraction of tracks reconstructed by MuTr-FEE, but not associated with MuTRG-FEE trigger fire can be considered as inefficiency of MuTRG-FEE. Association between hit location of MuTr-FEE and MuTRG-FEE is also required in this procedure to exclude accidental coincidence. Data set accumulated by the conventional MuID&BBC trigger was used for the efficiency evaluation.

Fig. 31 shows the efficiency for tracks as a function of the track momentum measured by the South muon arm in the 2011 RHIC Run.[4] The momentum thresholds for the track, which

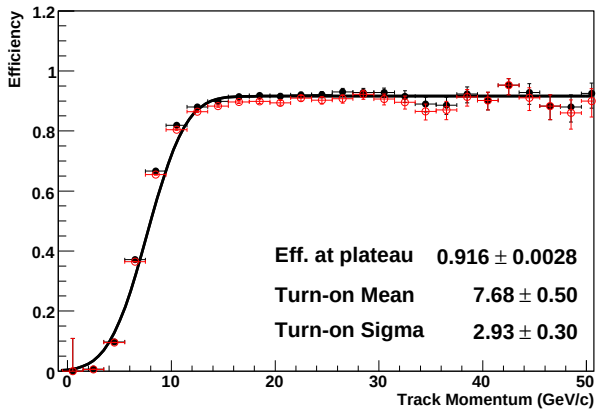



Figure 31: The track efficiency measured at proton-proton collisions in the 2011 RHIC Run. Black points are obtained by making association of tracks measured by MuTr and MuTRG-FEE hits in the offline analysis (See text). Red points require the online LL1 fire in addition to the offline association of MuTr tracks and MuTRG-FEE hits.

is represented by turn-on-point of the efficiency, are 7.7 GeV/$c$ and 12.6 GeV/$c$ in the total momentum for the South and North muon arm, respectively. As designed to be, MuTRG-FEE shows insensitivity to the low momentum tracks where backgrounds dominate and successfully raised momentum threshold of 2.8 GeV/$c$ provided by MuID. The new thresholds are on the other hand, low enough to be the region where $W$ signal becomes dominant. The lower threshold in the South arm compared to the North arm is due to shorter flight path length for the same magnetic field strength as the North arm.

The measured efficiency at plateau is 92 % for the South muon arm, as shown as filled-circle points in Fig. 31, and 87 % for the North muon arm. The source of the inefficiency is evaluated with data and summarized in Table 6. We must note that significant fraction of the high-momentum track samples reconstructed by MuTr must not be real, but so-called fake tracks, taking into account what one expects from cross sections of true high-momentum muon sources. Such the excess is most likely dominated by mis-reconstructed tracks of muons from hadron decays in the volume of MuTr and accidental coincidence of noise or multiple tracks. Somewhat better efficiency for the real high-momentum muons is expected. Unfortunately we do not have enough sample of true high-momentum muons to evaluate the efficiency performance because of smallness of their cross section. Instead, we confirmed the track efficiency of better than 96 % at high-momentum region in the measurements with cosmic ray.

| | South | North |
|---|---|---|
| Intrinsic inefficiency | 1 % | 2 % |
| AND2 for Station-1 | 2 % | 2 % |
| Timing cut of 3 beam clock window | 4 % | 5 % |
| Clustering | 2 % | 4 % |

Table 6: Sources of the inefficiency. Source of the intrinsic inefficiency includes threshold applied signal pulse height. Impurity of the selected tracks for the evaluation is also considered as a part of the intrinsic inefficiency.

To obtain the efficiency results of filled-circle points in Fig. 31, only MuTr and MuTRG-FEE hit information recorded by DCM with MuID&BBC trigger were utilized in the offline analysis (See Fig 4). In the real data taking, events must be triggered by MuTRG-FEE signal through the LL1 module. The points with open circle in Fig. 31, displays the MuTRG-FEE efficiency including the operating rate of the LL1 module. From this data, the LL1 operating rate was evaluated to be 98 % in the 2011 RHIC Run.

### *5.4. Rejection power*

Another important concern, as well as the efficiency, to evaluate the performance of the trigger is the rejection power. The rejection power is defined as the ratio of the BBC trigger rate divided by the rate of the trigger of focus. The rejection power of the new $W$ trigger is described as follows.

$$\text{Rejection Power} \equiv \frac{\text{Rate of MuTRG} - \text{FEE\&BBC\&MuID trigger}}{\text{Rate of BBC trigger}} \quad (1)$$

Fig. 32 shows rejection power of the MuID trigger and the MuTRG-FEE trigger as a function of the BBC trigger rate.

[4]The efficiencies shown here do not include inefficiency from MuID and BBC.

The curve guides the required rejection capability of the high-momentum muon trigger in order to fit trigger rate to be in the assigned bandwidth limit of PHENIX DAQ of 2 kHz for muon arms.

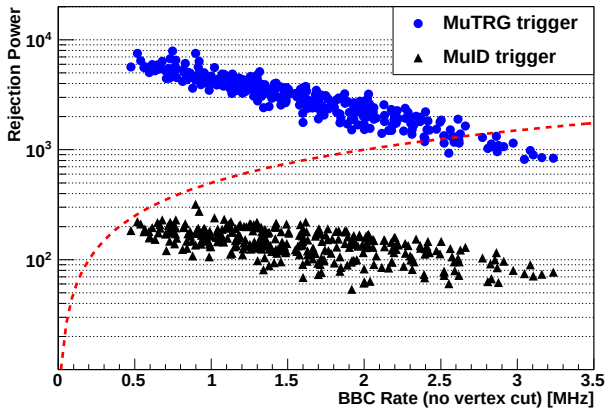



Figure 32: Rejection power as a function of BBC trigger rate. The curve indicates the boundary of the DAQ bandwidth of 2 kHz.

As can be seen from the figure, MuTRG-FEE strengthen the rejection power by factor of 10 to 40 compared to the conventional MuID trigger and kept the rejection power sufficiently high for the most of the case except for the very high luminosity period, i.e. BBC rate > 3 MHz. The measured rejection power indicates degradation of the trigger performance depending on the beam luminosity. As possible reasons of the luminosity dependence, we consider

- Degradation of MuID trigger rejection power. MuID suffers from ringing noise which generate fake triggers. Such fake triggers starts to make coincidence with beam collisions at high luminosity condition.
- Signal cross talk of MuTr over anode wires. It create fake hits after 30 $\mu$sec at the timing of signal undershoot and generate fake triggers. The effect is severe at high luminosity condition.
- Worse beam condition. The beam background is anticipated to be larger with high luminosity and it would generates fake triggers.

We expect that the trigger performance will be improved by making coincidence with RPC trigger which works in high rate condition.

## 6. Summary

We have implemented new electronics to existing signal readout system of muon tracking chambers. The new electronics digitize and process small fraction of the signal charge fast enough before the trigger decision in online, providing high momentum trigger based on coarse online tracking from a hit pattern. The new trigger makes the measurement of high momentum muons decayed from $W$-boson feasible which are overkilled by dominant low momentum backgrounds without it. The new electronics consist of MuTRG-ADTX, MuTRG-MRG, and MuTRG-DCMIF. MuTRG-ADTX takes care of signal split for the trigger and analog signal measurement. The back-end electronics MuTRG-MRG receives digitized signal from multiple MuTRG-ADTX boards and transmit these hit information to LL1 module for the trigger decision as well as sending the copy to DCM module via MuTRG-DCMIF for the offline performance analysis. The observed performance from the 2011 RHIC Run demonstrated 85 to 90 % trigger efficiencies for the detected high-momentum tracks which are expected to include significant fake tracks. Observed rejection power of new trigger combined with conventional MuID and BBC trigger was satisfactory for most of the 2011 RHIC Run except for very high luminosity period with BBC rate >3MHz. The rejection power will be improved by taking further combination with RPC trigger.

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## References

[1] C. Burrell and J. Soffer, Phys. Lett. B314, 132 1993.
[2] Conceptual Design Report for a Fast Muon Trigger (2007). R. Towell, Nucl. Instrum. Methods A602, 705 (2009).
[3] Technical Design Report on Amplifier-Discriminator board and Data Transfer board for the MuTr FEE upgrade (2008).
[4] I. Alekseev et al., Nucl. Instrum. Methods Phys. Res., Sect. A 499, 392 (2003)
[5] H. Akikawa et al., Nucl. Instrum. Methods Phys. Res., Sect. A 499, 537 (2003)
[6] K. Adcox et al., Nucl. Instrum. Methods Phys. Res., Sect. A 499, 469 (2003)
[7] S. S. Adler et al., Nucl. Instrum. Methods Phys. Res., Sect. A 499, 560 (2003)
[8] S. S. Adler et al., Nucl. Instrum. Methods Phys. Res., Sect. A 499, 593 (2003)
[9] M. Allen et al., Nucl. Instrum. Methods Phys. Res., Sect. A 499, 549 (2003)
[10] S. H. Aronson et al., Nucl. Instrum. Methods Phys. Res., Sect. A 499, 480 (2003)
[11] S. S. Adler et al. (PHENIX Collaboration), Phys. Rev. D 76, 092002 (2007)
[12] Xilinx Application Note 058 (XAPP058), Xilinx In-System Programming Using an Embedded Microcontroller

[13] G. Bunce, N. Saito, J. Soffer and W. Vogelsang, Ann. Rev. Nucl. Part. Sci. 50, 525 (2000)
[14] E. Iarocci, Nucl. Instrum. Meth. 217, 30 (1983)